

Table 3 summarizes EP910 features.

Feature	EP910-30	EP910-35	EP910-40	EP910T	EP910I
t_{PD}	30	35	40	30	12
Counter frequency	33 MHz	28 MHz	25 MHz	33 MHz	100 MHz
Pipeline data rates	41 MHz	37 MHz	32 MHz	41 MHz	100 MHz
Packages	44-pin JLCC 44-pin PLCC 40-pin CerDIP 40-pin PDIP	44-pin JLCC 44-pin PLCC 40-pin CerDIP 40-pin PDIP	44-pin JLCC 44-pin PLCC 40-pin CerDIP 40-pin PDIP	44-pin PLCC 40-pin PDIP	44-pin PLCC 40-pin CerDIP 40-pin PDIP

General Description

The Altera EP910 EPLD can implement up to 900 equivalent gates of SSI and MSI logic functions. The EP910 has 24 macrocells, 12 dedicated input pins, 24 I/O pins, and 2 global Clock pins (see Figure 12). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. CLK1 and CLK2 are the dedicated Clock inputs for the registers in macrocells 13 through 24 and 1 through 12, respectively.

Figure 12. EP910 Block Diagram

Numbers without parentheses are for DIP packages. Numbers in parentheses are for J-lead packages.

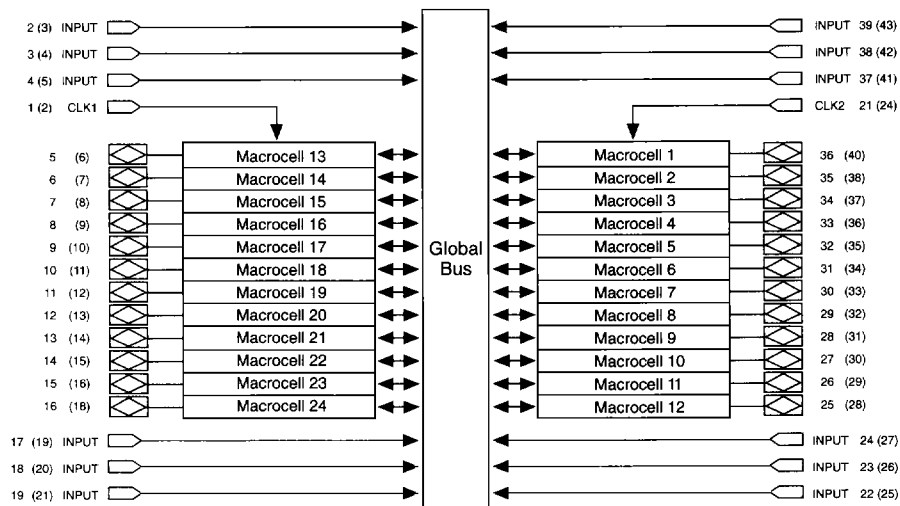
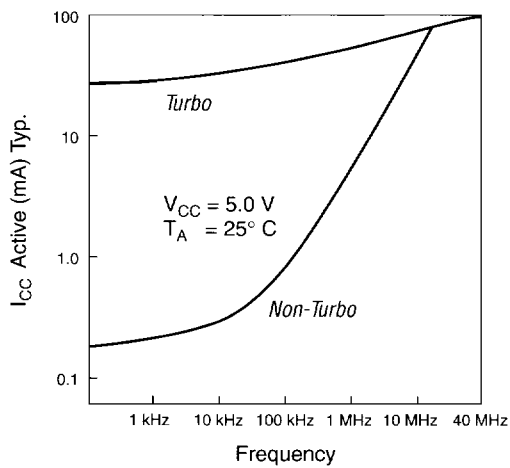


Figure 13 shows typical supply current (I_{CC}) versus frequency for EP910 devices.

Figure 13. EP910 I_{CC} vs. Frequency

EP910 EPLDs



EP910T EPLDs

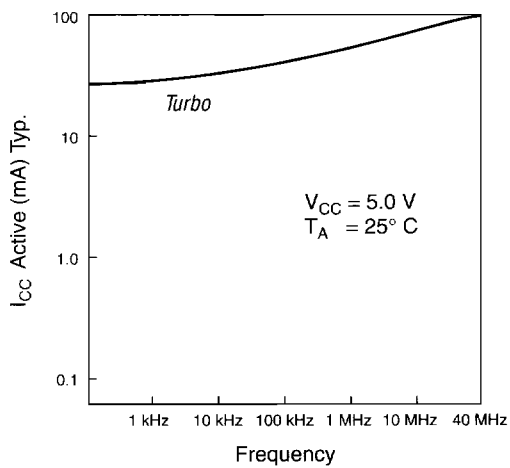
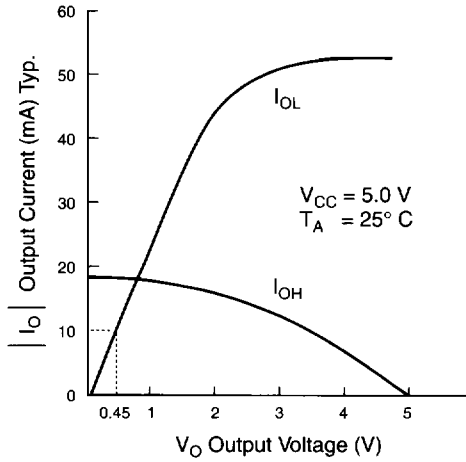


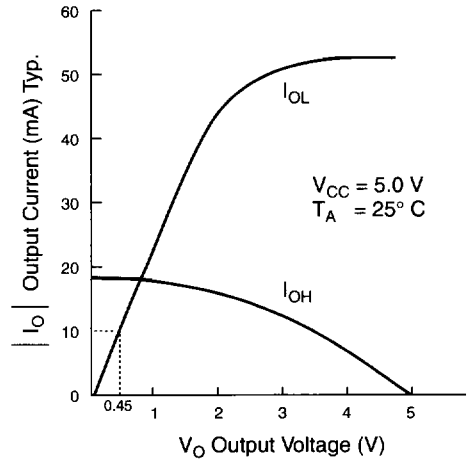
Figure 14 shows the output drive characteristics of EP910 I/O pins.

Figure 14. EP910 Output Drive Characteristics

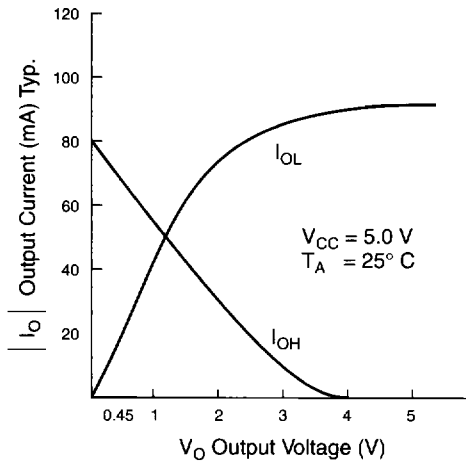
EP910 EPLDs



EP910T EPLDs



EP910I EPLDs



Absolute Maximum Ratings Note (1)

Symbol	Parameter	Conditions	EP910 EP910T		EP910I		Unit
			Min	Max	Min	Max	
V _{CC}	Supply voltage	Notes (2), (3)	-2.0	7.0	-2.0	7.0	V
V _I	DC input voltage	Notes (2), (3)	-2.0	7.0	-0.5	V _{CC} + 0.5	V
I _{MAX}	DC V _{CC} or GND current		-250	250			mA
I _{OUT}	DC output current, per pin		-25	25			mA
P _D	Power dissipation			1,200			mW
T _{STG}	Storage temperature	No bias	-65	150	-65	150	°C
T _{AMB}	Ambient temperature	Note (4)	-65	135	-10	85	°C

Recommended Operating Conditions Note (5)

Symbol	Parameter	Conditions	EP910 EP910T		EP910I		Unit
			Min	Max	Min	Max	
V _{CC}	Supply voltage	Note (6)	4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V _I	Input voltage		0	V _{CC}	0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
T _A	Operating temperature	For commercial use	0	70	0	70	°C
T _A	Operating temperature	For industrial use	-40	85			°C
T _C	Case temperature	For military use	-55	125			°C
t _R	Input rise time	Note (7)		100 (50)		500	ns
t _F	Input fall time	Note (7)		100 (50)		500	ns

DC Operating Conditions Notes (5), (8), (9)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IH}	High-level input voltage		2.0		V _{CC} + 0.3	V
V _{IL}	Low-level input voltage		-0.3		0.8	V
V _{OH}	High-level TTL output voltage	I _{OH} = -4 mA DC	2.4			V
V _{OH}	High-level CMOS output voltage	I _{OH} = -2 mA DC	3.84			V
V _{OL}	Low-level output voltage	I _{OL} = 4 mA DC			0.45	V
I _I	Input leakage current	V _I = V _{CC} or GND	-10		10	μA
I _{OZ}	Tri-state output leakage current	V _O = V _{CC} or GND	-10		10	μA

Capacitance Notes (8), (10)

Symbol	Parameter	Conditions	EP910 EP910T		EP910I		Unit
			Min	Max	Min	Max	
C_{IN}	Input pin capacitance	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		20		8	pF
C_{IO}	I/O pin capacitance	$V_{OUT} = 0\text{ V}$, $f = 1.0\text{ MHz}$		20		8	pF
C_{CLK1}	CLK1 pin capacitance	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		20		10	pF
C_{CLK2}	CLK2 pin capacitance	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$				12	pF

 I_{CC} Supply Current Notes (5), (8), (9)

Symbol	Parameter	Conditions	EP910			EP910T			EP910I			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC1}	V_{CC} supply current (non-turbo, standby)	$V_I = V_{CC}$ or GND, no load, Notes (11), (12)		20	150					60	150	μA
I_{CC2}	V_{CC} supply current (non-turbo, active)	$V_I = V_{CC}$ or GND, no load, $f = 1.0\text{ MHz}$, Note (12)		6	20					4	12	mA
I_{CC3}	V_{CC} supply current (turbo, active)			45	80 (100)		80	115		120	150	mA

Notes to tables:

- See *Operating Requirements for Altera Devices* in this data book.
- Voltage with respect to ground.
- For EP910 and EP910T EPLDs, the minimum DC input is -0.3 V ; for EP910I EPLDs, the minimum DC input is -0.5 V . During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
- Under bias. Extended temperature versions are also available.
- Numbers in parentheses are for industrial temperature versions.
- Maximum V_{CC} rise time for EP910 and EP910T devices = 50 ms ; for EP910I devices, maximum V_{CC} rise time is unlimited with monotonic rise.
- For all Clocks: t_R and $t_F = 100\text{ ns}$ (50 ns for military- and industrial-temperature-range versions).
- Operating conditions: $V_{CC} = 5\text{ V} \pm 5\%$, $T_A = 0^\circ\text{ C}$ to 70° C for commercial use.
 $V_{CC} = 5\text{ V} \pm 10\%$, $T_A = -40^\circ\text{ C}$ to 85° C for industrial use.
- Typical values are for $T_A = 25^\circ\text{ C}$ and $V_{CC} = 5\text{ V}$.
- For EP910 and EP910T devices: capacitance measured at 25° C ; sample-tested only; Clock-pin capacitance for dedicated Clock inputs only; pin 21 (high-voltage pin during programming) has a maximum capacitance of 60 pF . Values for EP910I devices are evaluated during initial characterization and design modifications.
- When the Turbo Bit is not set (non-turbo mode), an EP910I device will enter standby mode if no logic transitions occur for 75 ns after the last transition.
- Measured with a device programmed as a 24-bit counter.

AC Operating Conditions: EP910 Notes (1), (2)

Symbol	Parameter	Conditions	EP910-30 EP910T-30		EP910-35		EP910-40		Non-Turbo Adder	Unit
			Min	Max	Min	Max	Min	Max	Note (3)	
t _{PD1}	Input to non-registered output	C1 = 35 pF		30		35		40	30	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		33		38		43	30	ns
t _{PZx}	Input to output enable	C1 = 35 pF		30		35		40	30	ns
t _{PXZ}	Input to output disable	C1 = 5 pF, Note (4)		30		35		40	30	ns
t _{CLR}	Asynchronous output clear time	C1 = 35 pF		33		38		43	30	ns
t _{IO}	I/O input pad and buffer delay			3		3		3	0	ns
f _{MAX}	Maximum frequency	Note (5)	41.7		37.0		32.3		0	MHz
t _{SU}	Global clock input setup time		24		27		31		30	ns
t _H	Global clock input hold time		0		0		0		0	ns
t _{CH}	Global clock high time		12		13		15		0	ns
t _{CL}	Global clock low time		12		13		15		0	ns
t _{CO1}	Global clock to output delay			18		21		24	0	ns
t _{CNT}	Global clock minimum clock period			30		35		40	0	ns
f _{CNT}	Global clock internal maximum frequency	Note (6)	33.3		28.6		25.0		0	MHz
t _{ASU}	Array clock input setup time		10		10		10		30	ns
t _{AH}	Array clock input hold time		15		15		15		0	ns
t _{ACH}	Array clock high time		15		16		17		0	ns
t _{ACL}	Array clock low time		15		16		17		0	ns
t _{ACO1}	Array clock to output delay			33		38		43	30	ns
t _{ACNT}	Array clock minimum clock period			30		35		40	0	ns
f _{ACNT}	Array clock internal maximum frequency	Note (6)	33.3		28.6		25.0		0	MHz

Notes to tables:

- Operating conditions: $V_{CC} = 5\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C for commercial use.
 $V_{CC} = 5\text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 85°C for industrial use.
- See *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* for additional internal timing parameters.
- See "Turbo Bit" on page 336 of this data sheet. EP910T devices have no non-turbo mode.
- Sample-tested only for an output change of 500 mV.
- The f_{MAX} values represent the highest frequency for pipelined data.
- Measured with a device programmed as a 24-bit counter. I_{CC} measured at 0°C .

AC Operating Conditions: EP910I Notes (1), (2)

Symbol	Parameter	EP910I-12		EP910I-15		EP910I-25		Non-Turbo Adder	Unit
		Min	Max	Min	Max	Min	Max	Note (3)	
t _{PD1}	Input to non-registered output, Note (4)		12		15		25	40	ns
t _{PZX}	Input to output enable, Note (5)		15		18		28	40	ns
t _{PXZ}	Input to output disable, Note (5)		15		18		28	40	ns
t _{CLR}	Asynchronous output clear time		15		18		28	40	ns
f _{MAX}	Global clock maximum frequency	100		83.3		50		0	MHz
t _{SU}	Global clock input setup time	8		11		16		40	ns
t _H	Global clock input hold time	0		0		0		0	ns
t _{CH}	Global clock high time	5		6		10		0	ns
t _{CL}	Global clock low time	5		6		10		0	ns
t _{CO}	Global clock to output delay, Note (6)		8		9		14	0	ns
t _{CNT}	Global clock minimum clock period		13		15		25	40	ns
f _{CNT}	Global clock internal maximum frequency, Note (6)	76.9		66.6		40		0	MHz
t _{ASU}	Array clock input setup time	3		4		8		40	ns
t _{AH}	Array clock input hold time	6		7		8			ns
t _{ACH}	Array clock high time	6		7.5		12.5			ns
t _{ACL}	Array clock low time	6		7.5		12.5			ns
t _{ACO1}	Array clock to output delay, Note (6)		16		18		28	40	ns
t _{ACNT}	Array clock minimum clock period		13		15		25	40	ns
f _{ACNT}	Array clock internal maximum frequency, Note (6)	76.9		66.6		40			MHz

Notes to tables:

- Operating conditions: $V_{CC} = 5\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C for commercial use.
 $V_{CC} = 5\text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to 85°C for industrial use.
- See *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* for additional internal timing parameters.
- If the device is inactive for more than 75 ns while operated in non-turbo mode, increase time by amount shown. See "Turbo Bit" on page 336 of this data sheet.
- Measured with eight outputs switching.
- The t_{PZX} and t_{PXZ} parameters are measured at $\pm 0.5\text{ V}$ from steady-state voltage as driven by specified output load.
- Measured with device programmed as a 24-bit counter.