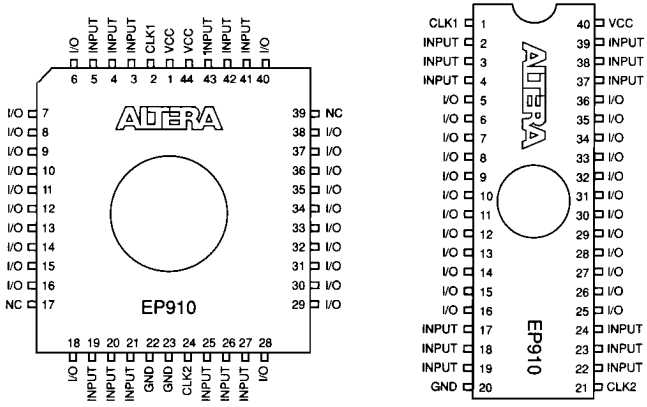
Features

- High-performance, 24-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 30, 35, and 40 ns
  - Counter frequencies up to 33 MHz
  - Pipelined data rates up to 41 MHz
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- Pin-, function-, and programming file-compatible with Altera's EP910A and EP910T EPLDs
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 21):
  - 44-pin J-lead chip carrier (JLCC and PLCC)
  - 40-pin dual in-line package (CerDIP and PDIP)

Figure 21. EP910 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



44-Pin J-Lead 40-Pin DIP

General Description

The Altera EP910 EPLD can implement up to 900 equivalent gates of SSI and MSI logic functions. The EP910 has 24 macrocells, 12 dedicated input pins, 24 I/O pins, and 2 global Clock pins (see Figure 22). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. CLOCK1 and CLOCK2 are the dedicated Clock inputs for the registers in macrocells 13 through 24 and 1 through 12, respectively.

Figure 22. EP910 Block Diagram

Numbers without parentheses are for DIP packages. Numbers in parentheses are for J-lead packages.

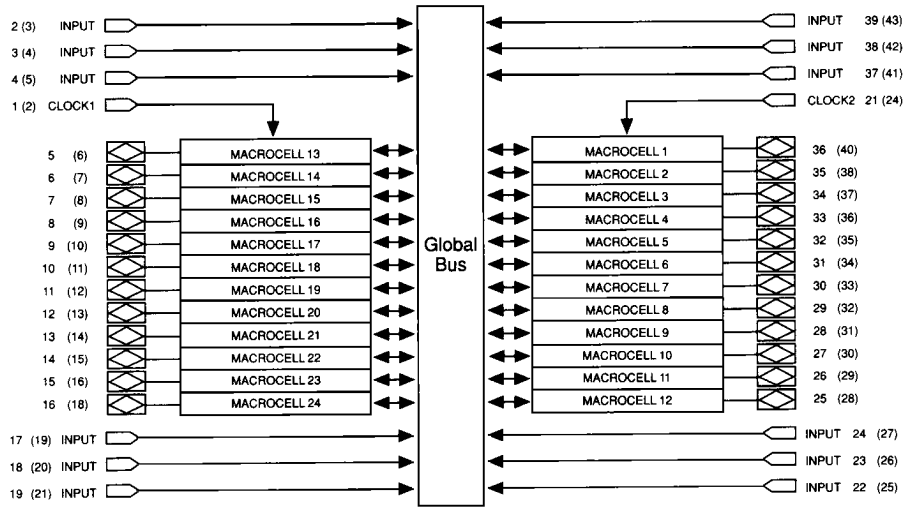
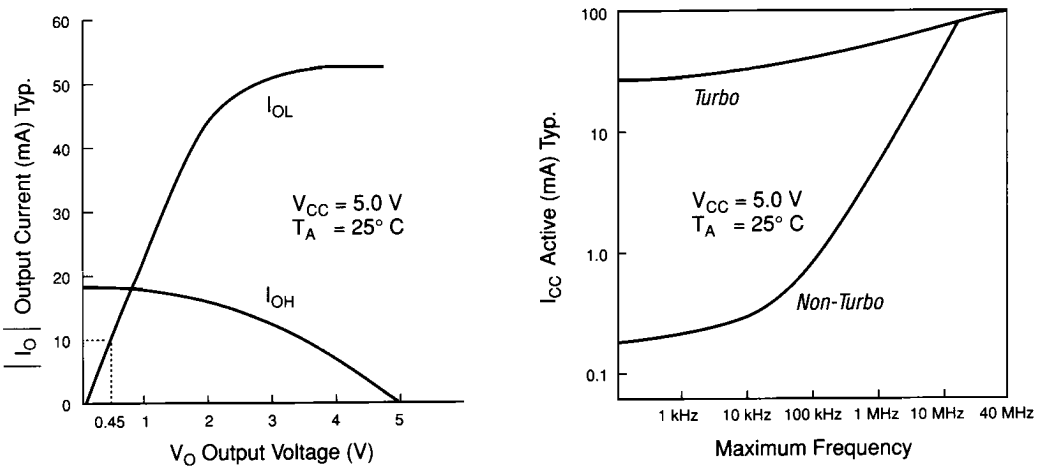


Figure 23 shows the output drive characteristics of EP910 I/O pins and typical supply current (I_{CC}) versus frequency for the EP910 EPLD.

Figure 23. EP910 Maximum Output Drive Characteristics and I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–250	250	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1200	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (2)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time	*Note (3)*		100 (50)	ns
t_F	Input fall time			100 (50)	ns

DC Operating Conditions *Notes (2), (4), (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, No load, *Notes (6), (7)*		20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Note (7)*		6	20	mA
I_{CC3}	V_{CC} supply current (turbo, active)			45	80 (100)	mA

Capacitance *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (5)*

			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		30		35		40	30	ns
t_{PD2}	I/O input to non-registered output			33		38		43	30	ns
t_{PZX}	Input to output enable			30		35		40	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (10)*		30		35		40	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		33		38		43	30	ns
t_{IO}	I/O input pad and buffer delay			3		3		3	0	ns

Global Clock Mode			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*Note (11)*	41.7		37.0		32.3		0	MHz
t_{SU}	Input setup time		24		27		31		30	ns
t_{H}	Input hold time		0		0		0		0	ns
t_{CH}	Clock high time		12		13		15		0	ns
t_{CL}	Clock low time		12		13		15		0	ns
t_{CO1}	Clock to output delay			18		21		24	0	ns
t_{CNT}	Minimum clock period			30		35		40	0	ns
f_{CNT}	Internal maximum frequency	*Note (7)*	33.3		28.6		25.0		0	MHz

Array Clock Mode			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*Note (11)*	33.3		31.3		29.4		0	MHz
t_{ASU}	Input setup time		10		10		10		30	ns
t_{AH}	Input hold time		15		15		15		0	ns
t_{ACH}	Clock high time		15		16		17		0	ns
t_{ACL}	Clock low time		15		16		17		0	ns
t_{ACO1}	Clock to output delay			33		38		43	30	ns
t_{ACNT}	Minimum clock period			30		35		40	0	ns
f_{ACNT}	Internal maximum frequency	*Note (7)*	33.3		28.6		25.0		0	MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature versions.
(3) For all Clocks: t_R and t_F = 100 ns (50 ns for military and industrial temperature versions).
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) When the Turbo Bit is not set (non-turbo mode), an EP910 EPLD will enter standby mode if no logic transitions occur for 100 ns (after the last transition).
(7) Measured with a device programmed as a 24-bit counter. I_{CC} measured at 0° C.
(8) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. Pin 21 (high-voltage pin during programming) has a maximum capacitance of 60 pF.
(9) See "Turbo Bit" earlier in this data sheet.
(10) Sample-tested only for an output change of 500 mV.
(11) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP910-30, EP910-35, EP910-40
Industrial Temp.	(–40° C to 85° C)	EP910-35, EP910-40
Military Temp.	(–55° C to 125° C)	Consult factory