Features

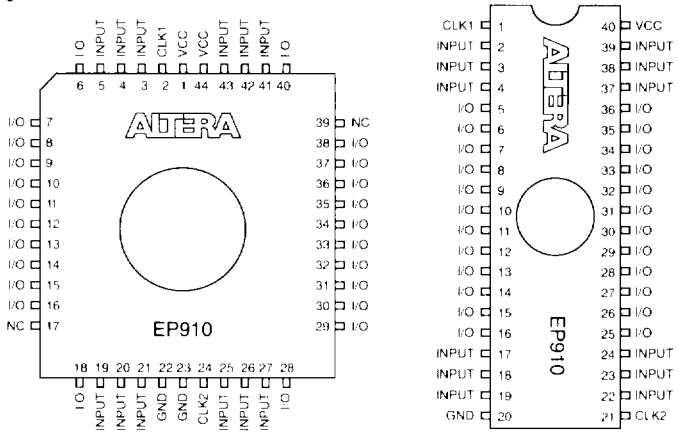
- High-performance 24-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 30 ns
  - Counter frequencies up to 33 MHz
  - Pipelined data rates up to 41 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP910A and EP910T EPLDs
- 100% generically testable to provide 100% programming yield
- Available in windowed ceramic and one-time-programmable (OTP) plastic chip carrier packages
  - 44-pin J-lead chip carrier (JLCC and PLCC)
  - 40-pin dual in-line package (CerDIP and PDIP)
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP910 Erasable Programmable Logic Device (EPLD) can implement up to 900 equivalent gates of SSI and MSI logic. It is available in windowed ceramic or OTP plastic 40-pin DIP and 44-pin J-lead chip carrier packages. See Figure 7.

Figure 7. EP910 Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–250	250	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1200	mW
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*See Note (2)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	°C
T_A	Operating temperature	For industrial use	–40	85	°C
T_C	Case temperature	For military use	–55	125	°C
t_R	Input rise time	*See Note (3)*		100 (50)	ns
t_F	Input fall time	*See Note (3)*		100 (50)	ns

DC Operating Conditions

See Notes (2), (4), (5)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (non-turbo standby)	$V_I = V_{CC}$ or GND, No load, *See Note (6)*		20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (7)*		6	20	mA
I_{CC3}	V_{CC} supply current (turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (7)*		45	80 (100)	mA

Capacitance *See Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (5)*

			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	*Note (9)*	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		30		35		40	30	ns
t_{PD2}	I/O input to non-registered output			33		38		43	30	ns
t_{PZX}	Input to output enable			30		35		40	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *See Note (10)*		30		35		40	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		33		38		43	30	ns
t_{IO}	I/O input pad and buffer delay			3		3		3	0	ns

Global Clock Mode			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	*Note (9)*	Unit
f_{MAX}	Maximum frequency	*See Note (11)*	41.7		37.0		32.3		0	MHz
t_{SU}	Input setup time		24		27		31		30	ns
t_{H}	Input hold time		0		0		0		0	ns
t_{CH}	Clock high time		12		13		15		0	ns
t_{CL}	Clock low time		12		13		15		0	ns
t_{CO1}	Clock to output delay			18		21		24	0	ns
t_{CNT}	Minimum clock period			30		35		40	0	ns
f_{CNT}	Internal maximum frequency	*See Note (7)*	33.3		28.6		25.0		0	MHz

Array Clock Mode			EP910-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	*Note (9)*	Unit
f_{MAX}	Maximum frequency	*See Note (11)*	33.3		31.3		29.4		0	MHz
t_{ASU}	Input setup time		10		10		10		30	ns
t_{AH}	Input hold time		15		15		15		0	ns
t_{ACH}	Clock high time		15		16		17		0	ns
t_{ACL}	Clock low time		15		16		17		0	ns
t_{ACO1}	Clock to output delay			33		38		43	30	ns
t_{ACNT}	Minimum clock period			30		35		40	0	ns
f_{ACNT}	Internal maximum frequency	*See Note (7)*	33.3		28.6		25.0		0	MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature versions.
(3) For all clocks: t_R and t_F = 100 ns (50 ns).
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) When in non-turbo mode, an EPLD will automatically enter standby mode if logic transitions do not occur (approximately 100 ns after the last transition).
(7) Measured with a device programmed as a 24-bit counter.
(8) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. Pin 21 (high-voltage pin during programming) has a maximum capacitance of 60 pF.
(9) See "Turbo Bit" earlier in this data sheet.
(10) Sample-tested only for an output change of 500 mV.
(11) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP910-30, EP910-35, EP910-40
Industrial	(–40° C to 85° C)	EP910-35, EP910-40
Military	(–55° C to 125° C)	EP910-40

Note: Only military-temperature-range devices are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera's Marketing Department at (408) 984-2800. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

Figure 8 shows the output drive characteristics for EP910 I/O pins and typical supply current versus frequency for the EP910 EPLD.

Figure 8. EP910 Output Drive Characteristics and I_{CC} vs. Frequency