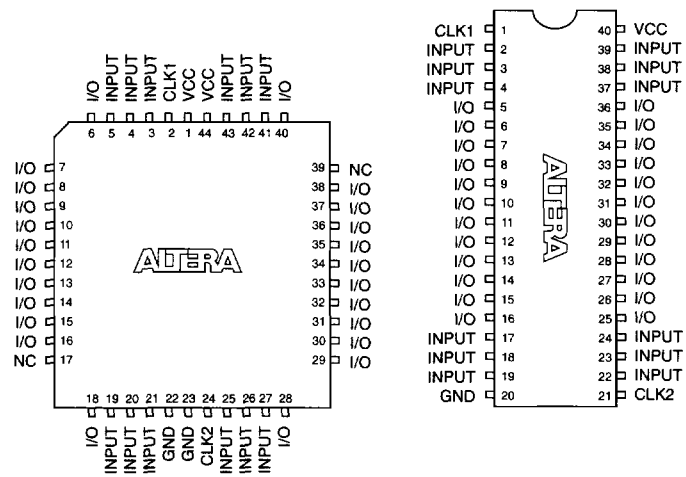
Features

- High-performance, 24-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as fast as 12 ns
  - Counter frequencies of up to 76.9 MHz
  - Pipelined data rates of up to 125 MHz
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- EP910 and EP910I devices are pin-, function-, and programming file-compatible
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in the following packages (see Figure 11)
  - 44-pin plastic J-lead chip carrier (PLCC)
  - 40-pin ceramic and plastic dual in-line packages (CerDIP and PDIP)

Figure 11. EP910 Package Pin-Out Diagrams

Package outlines are not drawn to scale. Windows in ceramic packages only.



44-Pin PLCC

EP910
EP910I

40-Pin DIP

EP910
EP910I

General Description

Altera EP910 devices can implement up to 450 usable gates of SSI and MSI logic functions. EP910 devices have 24 macrocells, 12 dedicated input pins, 24 I/O pins, and 2 global clock pins (see Figure 12). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. The CLK1 and CLK2 signals are the dedicated clock inputs for the registers in macrocells 13 through 24 and 1 through 12, respectively.

Figure 12. EP910 Block Diagram

Numbers without parentheses are for DIP packages. Numbers in parentheses are for J-lead packages.

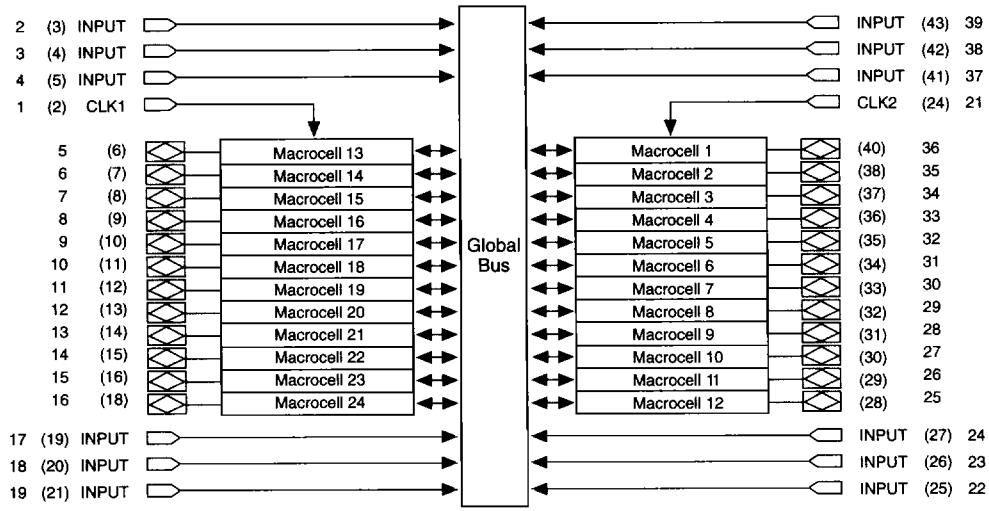


Figure 13 shows the typical supply current (I_{CC}) versus frequency of EP910 devices.

Figure 13. I_{CC} vs. Frequency of EP910 Devices

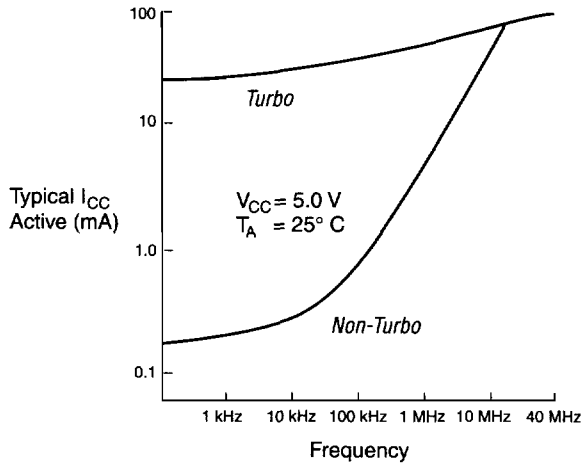
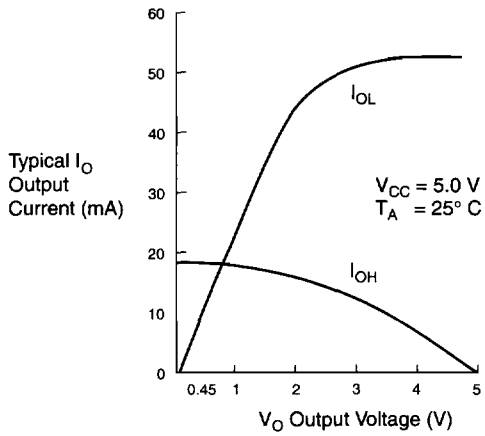


Figure 14 shows the typical output drive characteristics of EP910 devices.

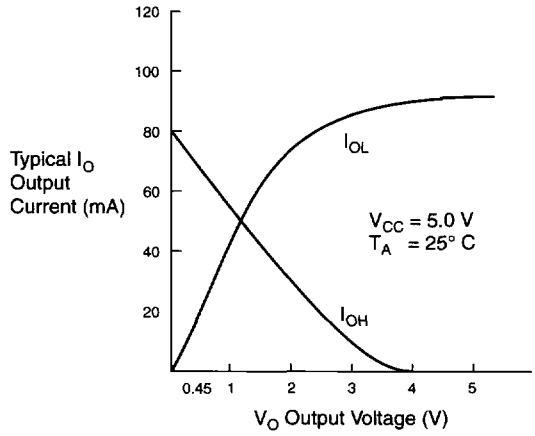
Figure 14. Output Drive Characteristics of EP910 Devices

Drive characteristics may exceed shown curves.

EP910 EPLDs



EP910I EPLDs



Operating Conditions

Tables 14 through 18 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for EP910 and EP910I devices.

Table 14. EP910 & EP910I Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	EP910		EP910I		Unit
			Min	Max	Min	Max	
V_{CC}	Supply voltage	With respect to ground *(3)*	–2.0	7.0	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	–0.5	V_{CC} + 0.5	V
I_{MAX}	DC V_{CC} or ground current		–250	250			mA
I_{OUT}	DC output current, per pin		–25	25			mA
T_{STG}	Storage temperature	No bias	–65	150	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150		150	° C
		Plastic packages, under bias		135		135	° C

Table 15. EP910 & EP910I Device Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	EP910		EP910I		Unit
			Min	Max	Min	Max	
V_{CC}	Supply voltage	*(4)*	4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V_I	Input voltage		–0.3	V_{CC} + 0.3	–0.3	V_{CC} + 0.3	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	0	70	° C
		For industrial use	–40	85			° C
t_R	Input rise time	*(5)*		100 (50)		500	ns
t_F	Input fall time	*(5)*		100 (50)		500	ns

Table 16. EP910 & EP910I Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC *(8)*	2.4		V
	High-level CMOS output voltage	I_{OH} = –0.6 mA DC *(8), (9)*	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC *(8)*		0.45	V
I_I	I/O leakage current of dedicated input pins	V_I = V_{CC} or ground	–10	10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or ground	–10	10	µA

Table 17. EP910 & EP910I Device Capacitance *Note (6)*

Symbol	Parameter	Conditions	EP910		EP910I		Unit
			Min	Max	Min	Max	
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20		8	pF
C_{CLK1}	CLK1 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		10	pF
C_{CLK2}	CLK2 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		60		12	pF

Table 18. EP910 & EP910I Device I_{CC} Supply Current *Notes (2), (6), (7)*

Symbol	Parameter	Conditions	EP910			EP910I			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	$V_I = V_{CC}$ or ground, no load *(10), (11)*		20	150		60	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	$V_I = V_{CC}$ or ground, no load, f = 1.0 MHz *(10), (11)*		6	20		4	12	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	$V_I = V_{CC}$ or ground, no load, f = 1.0 MHz *(11)*		45	80 (100)		120	150	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Numbers in parentheses are for industrial-temperature-range devices.
(3) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V (EP910) or –0.5 V (EP910I) or overshoot to 7.0 V (EP910) or V_{CC} + 0.5 V (EP910I) for input currents less than 100 mA and periods less than 20 ns.
(4) Maximum V_{CC} rise time for EP910 devices = 50 ms; for EP910I devices, maximum V_{CC} rise time is unlimited with monotonic rise.
(5) For all clocks: t_R and t_F = 100 ns (50 ns for the industrial-temperature-range version).
(6) These values are specified in Table 15 on page 770.
(7) The device capacitance is measured at 25° C and is sample-tested only.
(8) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL output current.
(9) This parameter does not apply to EP910I devices.
(10) When the Turbo Bit option is not set (non-Turbo mode), an EP910 device will enter standby mode if no logic transitions occur for 100 ns after the last transition, and an EP910I device will enter standby mode if no logic transitions occur for 75 ns after the last transition.
(11) Measured with a device programmed as a 24-bit counter.

Tables 19 and 20 show the timing parameters for EP910 devices.

Table 19. EP910 External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	EP910-30		EP910-35		EP910-40		Non-Turbo Adder *(3)*	Unit
			Min	Max	Min	Max	Min	Max		
t_{PD1}	Input to non-registered output	C1 = 35 pF		30.0		35.0		40.0	30.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		33.0		38.0		43.0	30.0	ns
t_{PZX}	Input to output enable	C1 = 35 pF		30.0		35.0		40.0	30.0	ns
t_{PXZ}	Input to output disable	C1 = 5 pF *(4)*		30.0		35.0		40.0	30.0	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		33.0		38.0		43.0	30.0	ns
f_{MAX}	Maximum frequency	*(5)*	41.7		37.0		32.3		0.0	MHz
t_{SU}	Global clock input setup time		24.0		27.0		31.0		30.0	ns
t_{H}	Global clock input hold time		0.0		0.0		0.0		0.0	ns
t_{CH}	Global clock high time		12.0		13.0		15.0		0.0	ns
t_{CL}	Global clock low time		12.0		13.0		15.0		0.0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		18		21.0		24.0	0.0	ns
t_{CNT}	Global clock minimum clock period	*(6)*		30.0		35.0		40.0	0.0	ns
f_{CNT}	Maximum internal global clock frequency	*(6)*	33.3		28.6		25.0		0.0	MHz
t_{ASU}	Array clock input setup time		10.0		10.0		10.0		30.0	ns
t_{AH}	Array clock input hold time		15.0		15.0		15.0		0.0	ns
t_{ACH}	Array clock high time		15.0		16.0		17.0		0.0	ns
t_{ACL}	Array clock low time		15.0		16.0		17.0		0.0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(7)*	1.0		1.0		1.0			ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		33.0		38.0		43.0	30.0	ns
t_{ACNT}	Array clock minimum clock period			30.0		35.0		40.0	0.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(6)*	33.3		28.6		25.0		0.0	MHz

Table 20. EP910 Internal Timing Parameters

Symbol	Parameter	Condition	EP910-30		EP910-35		EP910-40		Unit
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			9.0		10.0		13.0	ns
t_{IO}	I/O input pad and buffer delay			3.0		3.0		3.0	ns
t_{LAD}	Logic array delay			14.0		16.0		17.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		7.0		9.0		10.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		7.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7.0		9.0		10.0	ns
t_{SU}	Register setup time		12.0		13.0		15.0		ns
t_{H}	Register hold time		12.0		12.0		12.0		ns
t_{IC}	Array clock delay			17.0		19.0		20.0	ns
t_{ICS}	Global clock delay			2.0		2.0		1.0	ns
t_{FD}	Feedback delay			4.0		6.0		8.0	ns
t_{CLR}	Register clear time			17.0		19.0		20.0	ns

Notes to tables:

(1) These values are specified in Table 15 on page 770.
(2) See *Application Note 78 (Understanding MAX 5000 & Classic Timing)* in this data book for more information on Classic timing parameters.
(3) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.
(4) Sample-tested only for an output change of 500 mV.
(5) The f_{MAX} values represent the highest frequency for pipelined data.
(6) Measured with a device programmed as a 24-bit counter.
(7) Sample-tested only. This parameter is a guideline based on extensive device characterization and applies for both global and array clocking.

Tables 21 and 22 show the timing parameters for EP910I devices.

Table 21. EP910I External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	EP910I-12		EP910I-15		EP910I-25		Non-Turbo Adder	Unit
			Min	Max	Min	Max	Min	Max	*(3)*	
t_{PD1}	Input to non-registered output	C1 = 35 pF		12.0		15.0		25.0	40.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		12.0		15.0		25.0	40.0	ns
t_{PZX}	Input to output enable	C1 = 35 pF		15.0		18.0		28.0	40.0	ns
t_{PXZ}	Input to output disable	C1 = 35 pF *(4)*		15.0		18.0		28.0	40.0	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15.0		18.0		28.0	40.0	ns
f_{MAX}	Global clock maximum frequency	*(5)*	125.0		100.0		62.5		0.0	MHz
t_{SU}	Global clock input setup time		8.0		11.0		16.0		40.0	ns
t_{H}	Global clock input hold time		0.0		0.0		0.0		0.0	ns
t_{CH}	Global clock high time		5.0		6.0		10.0		0.0	ns
t_{CL}	Global clock low time		5.0		6.0		10.0		0.0	ns
t_{CO1}	Global clock to output delay			8.0		9.0		14.0	0.0	ns
t_{CNT}	Global clock minimum clock period	C1 = 35 pF		13.0		15.0		25.0	40.0	ns
f_{CNT}	Maximum internal global clock frequency	*(6)*	76.9		66.6		40.0		0.0	MHz
t_{ASU}	Array clock input setup time		3.0		4.0		8.0		40.0	ns
t_{AH}	Array clock input hold time		6.0		7.0		8.0			ns
t_{ACH}	Array clock high time		6.0		7.5		12.5			ns
t_{ACL}	Array clock low time		6.0		7.5		12.5			ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(7)*	1.0		1.0		1.0			ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		16.0		18.0		22.0	40.0	ns
t_{ACNT}	Array clock minimum clock period			13.0		15.0		25.0	40.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(6)*	76.9		66.6		40.0			MHz

Table 22. EP910I Internal Timing Parameters

Symbol	Parameter	Condition	EP910I-12		EP910I-15		EP910I-25		Unit
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			2.0		3.0		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.0		0.0		0.0	ns
t_{LAD}	Logic array delay			8.0		9.0		17.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		2.0		3.0		6.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5.0		6.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5.0		6.0		9.0	ns
t_{SU}	Register setup time		4.0		5.0		5.0		ns
t_{H}	Register hold time		4.0		6.0		11.0		ns
t_{IC}	Array clock delay			12.0		12.0		14.0	ns
t_{ICS}	Global clock delay			4.0		3.0		6.0	ns
t_{FD}	Feedback delay			1.0		1.0		3.0	ns
t_{CLR}	Register clear time			11.0		12.0		20.0	ns

Notes to tables:

(1) These values are specified in Table 15 on page 770.
(2) See *Application Note 78 (Understanding MAX 5000 & Classic Timing)* in this data book for information on internal timing parameters.
(3) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.
(4) Sample-tested only for an output change of 500 mV.
(5) The f_{MAX} values represent the highest frequency for pipelined data.
(6) Measured with the device programmed as a 24-bit counter.
(7) Sample-tested only. This parameter is a guideline based on extensive device characterization and applies for both global and array clocking.