



EP9001
Classic EPLD

March 1995, ver. 2

Data Sheet Supplement

This data sheet supplement should be used together with the *Classic Family Data Sheet*.

Features

- Formerly Intel's 5C090 device
- High-performance, 24-macrocell Classic EPLD
 - Combinatorial speeds with $t_{PD} = 50$ ns
 - Counter frequencies up to 20 MHz
 - Pipelined data rates up to 26.3 MHz
- Pin-, function-, and programming file-compatible with Altera's EP910 EPLDs
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable plastic packages:
 - 40-pin dual in-line packages (CerDIP and PDIP)
 - 44-pin plastic J-lead chip carrier (PLCC)

Absolute Maximum Ratings See Operating Requirements for Altera Devices in the current Altera *Data Book*.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply voltage	Note (1)	-2.0	7.0	V
V _I	DC input voltage	Notes (1), (2)	-0.5	V _{CC} + 0.5	V
T _{STG}	Storage temperature		-65	150	°C
T _{AMB}	Ambient temperature	Note (3)	-10	85	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply voltage		4.75	5.25	V
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
T _A	Operating temperature	For commercial use	0	70	°C
T _A	Operating temperature	For industrial use	-40	85	°C
t _R	Input rise time	Note (4)		500	ns
t _F	Input fall time	Note (4)		500	ns

DC Operating Conditions Note (5)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IH}	High-level input voltage	Note (6)	2.0		V _{CC} + 0.3	V
V _{IL}	Low-level input voltage	Note (6)	-0.3		0.8	V
V _{OH}	High-level output voltage	I _{OH} = -4 mA DC, V _{CC} = min	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 4 mA DC, V _{CC} = min			0.45	V
I _I	Input leakage current	V _{CC} = max, GND < V _{IN} < V _{CC}	-10		10	μA
I _{OZ}	Tri-state output off-state current	V _{CC} = max, GND < V _{OUT} < V _{CC}	-10		10	μA
I _{CC1}	V _{CC} supply current (non-turbo, standby)	V _{CC} = max, V _{IN} = V _{CC} or GND, Note (7)		50	150	μA
I _{CC2}	V _{CC} supply current (non-turbo, active)	V _{CC} = max, V _{IN} = V _{CC} or GND, no load, f _{IN} = 1 MHz, Note (8)		15	25	mA

Capacitance Note (5)

Symbol	Parameter	Conditions	Min	Max	Unit
C _{IN}	Input capacitance	V _{IN} = 0 V, f = 1.0 MHz		20	pF
C _{OUT}	Output capacitance	V _{OUT} = 0 V, f = 1.0 MHz		20	pF
C _{CLK1}	CLK1 pin capacitance	V _{IN} = 0 V, f = 1.0 MHz		20	pF
C _{CLK2}	CLK2 pin capacitance	V _{IN} = 0 V, f = 1.0 MHz		80	pF

AC Operating Conditions Note (5)

External Timing Parameters			EP9001-50		EP9001-60		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Note (9)	Unit
t_{PD1}	Input to non-registered output			45		55	25	ns
t_{PD2}	I/O input to non-registered output			50		60	25	ns
t_{PZX}	Input to output enable	Note (10)		50		60	25	ns
t_{PXZ}	Input to output disable	Note (10)		50		60	25	ns
t_{CLR}	Asynchronous output clear time			50		60	25	ns

Global Clock Mode			EP9001-50		EP9001-60		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Note (9)	Unit
f_{MAX}	Maximum frequency		26.3		21.7		0	MHz
t_{SU1}	Input setup time		36		43		25	ns
t_{SU2}	I/O setup time		38		46		25	ns
t_H	Input hold time		0		0		0	ns
t_{CH}	Clock high time		17.5		23		0	ns
t_{CL}	Clock low time		17.5		23		0	ns
t_{CO}	Clock to output delay			23		25	0	ns
t_{CNT}	Minimum clock period			50		60	25	ns
f_{CNT}	Internal maximum frequency		20		16.7		0	MHz

Array Clock Mode			EP9001-50		EP9001-60		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Note (9)	Unit
f_{MAX}	Maximum frequency		28.6		21.7		0	MHz
t_{ASU1}	Input setup time		10		10		25	ns
t_{ASU2}	I/O setup time		13		15		25	ns
t_{AH}	Input hold time		15		15		0	ns
t_{ACH}	Clock high time		17.5		23		25	ns
t_{ACL}	Clock low time		17.5		23		25	ns
t_{ACO}	Clock to output delay			48		59	25	ns
t_{ACNT}	Minimum clock period			50		60	25	ns
f_{ACNT}	Internal maximum frequency		20		16.7		0	MHz

Notes to tables:

- (1) Voltage is with respect to GND.
- (2) The minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to $+7.0$ V for periods less than 20 ns under no-load conditions.
- (3) This parameter is under bias. Extended temperature versions are also available.
- (4) For all Clocks: t_R and $t_F = 250$ ns (maximum).
- (5) Operating conditions: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{ V} \pm 5\%$ for commercial use.
 $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 5.0\text{ V} \pm 10\%$ for industrial use.
- (6) Absolute values with respect to device GND; all over- and undershoots due to system or tester noise are included.
- (7) When the Turbo Bit is not set (non-turbo mode), the device enters standby mode approximately 100 ns after the last input transition.
- (8) Measured with a device programmed as a 24-bit counter.
- (9) When the Turbo Bit is not set (non-turbo mode), the non-turbo adder values must be added to the appropriate AC parameter to determine worst-case timing.
- (10) The t_{pZX} and t_{pXZ} parameters are measured at ± 0.5 V from steady state voltage as driven by the output load specification; t_{pZX} is measured with $C_L = 5$ pF.

Ordering Information

Package	Speed Grade	Product Grade (1)	Ordering Code
40-pin CerDIP	-50	Commercial	EP9001DC-50
40-pin PDIP	-50	Commercial	EP9001PC-50
40-pin PDIP	-60	Commercial	EP9001PC-60
44-pin PLCC	-50	Commercial	EP9001LC-50
44-pin PLCC	-60	Commercial	EP9001LC-60
44-pin PLCC	-60	Industrial	EP9001LI-60

Note:

- (1) Operating temperature: 0°C to 70°C for commercial use.
 -40°C to 85°C for industrial use.

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