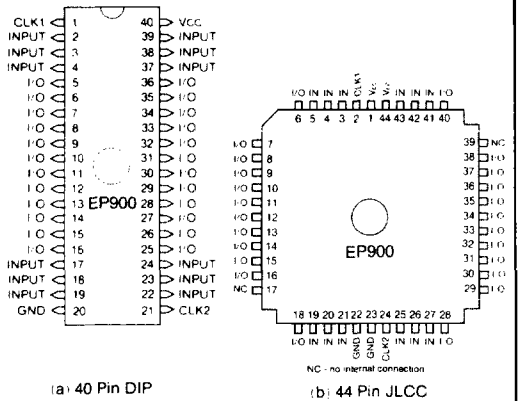
EP900 ERASABLE PROGRAMMABLE LOGIC DEVICE

FEATURES

- High density (over 900 gates) replacement for TTL and 74HC.
- Advanced CHMOS EPROM technology allows erasability and reprogrammability.
- High speed, t_{pd} = 30ns.
- "Zero Power" (typically 10μA standby)
- Asynchronous clocking of all registers or banked register operation from 2 synchronous clocks.
- 24 Macrocells with configurable I/O architecture allowing 36 inputs and 24 outputs.
- Programmable registers providing D, T, SR or JK flipflops with individual Asynchronous Clear control.
- 100% generically testable—provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Advanced software support featuring Schematic Capture, Interactive Netlist, Boolean Equation and State Machine design entry methods.
- Package options include both a 40 pin, 600 mil DIP and a 44 pin J-leaded chip carrier.

CONNECTION DIAGRAM



(a) 40 Pin DIP

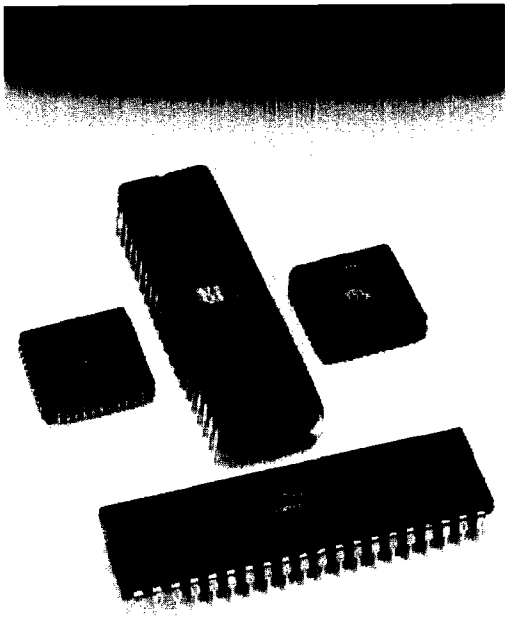
(b) 44 Pin JLCC

GENERAL DESCRIPTION

The ALTERA EP900 Erasable Programmable Logic Device may be used to implement over 900 equivalent gates of SSI and MSI logic, accommodating up to 36 inputs and 24 outputs all within a 40 pin DIP or 44 pin J-leaded chip carrier.

Each of the 24 Macrocells contains a programmable AND, fixed OR PLA structure which yields 8 product terms for logic implementation, and single product terms for Output Enable and Asynchronous Clear control functions.

The ALTERA proprietary programmable I/O architecture allows the EP900 user to program output and feedback paths for both combinatorial or registered operation, active high or active low.



REV. 2.0

For increased flexibility, the EP900 also includes programmable registers. Each of the 24 internal registers may be programmed to be a D, T, SR or JK flipflop. In addition, each register may be clocked asynchronously on an individual basis or synchronously on a banked register basis.

In addition to density and flexibility, the performance characteristics allow the EP900 to be used in the widest possible range of applications. The CHMOS EPROM technology reduces active power consumption to less than 20% of equivalent bipolar devices without a sacrifice in speed performance. This technology also facilitates 100% generic testability as well as UV erasability. As a result, designs and design modifications may be quickly implemented upon a given EP900 without the need for post programming testing.

Programming the EP900 is accomplished by using the ALTERA A+PLUS development software which supports schematic capture, netlist, state machine and Boolean equation design entry methods. Once the design is entered, A+PLUS automatically performs translation into logical equations, Boolean minimization, and design fitting directly to an EP900. The device may then be programmed to achieve customized working silicon within minutes at the designer's own desktop.

FUNCTIONAL DESCRIPTION

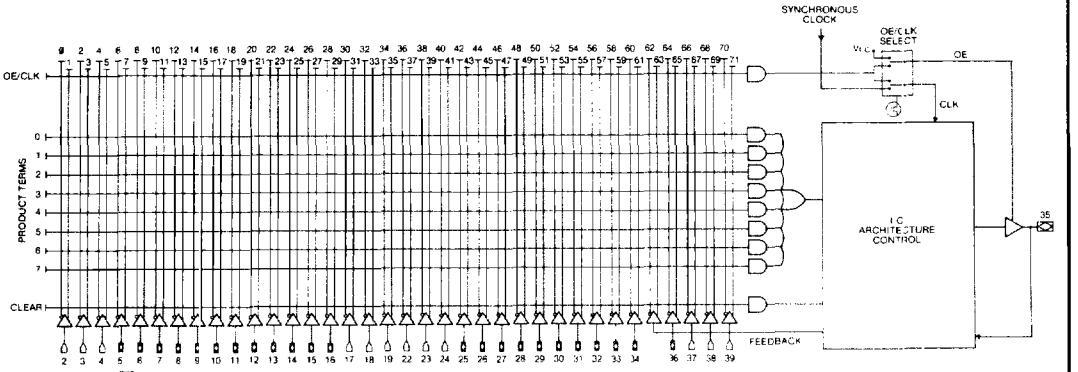
The EP900 is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM technology is utilized in order to configure connections in a programmable AND logic array. EPROM connections are also used to construct a revolutionary programmable I/O architecture which provides advanced functional capability for user programmable logic.

Externally, the EP900 provides 12 dedicated data inputs, 2 synchronous clock inputs and 24 I/O pins which may be configured for input, output or bi-directional operation.

Figure 1 shows the basic EP900 Macrocell while figure 2 shows the complete EP900 block diagram. The internal architecture is organized with the familiar sum of products (AND-OR) structure. Inputs to the programmable AND array (running vertically in Figure 1) come from the true and complement forms of: 1) the 12 dedicated data inputs and; 2) the 24 feedback signals originating from each of the 24 I/O architecture control blocks. The 72 input AND array encompasses 240 product terms, distributed equally among the EP900's 24 Macrocells. Each product term (running horizontally in Figure 1) represents a 72 input AND gate.

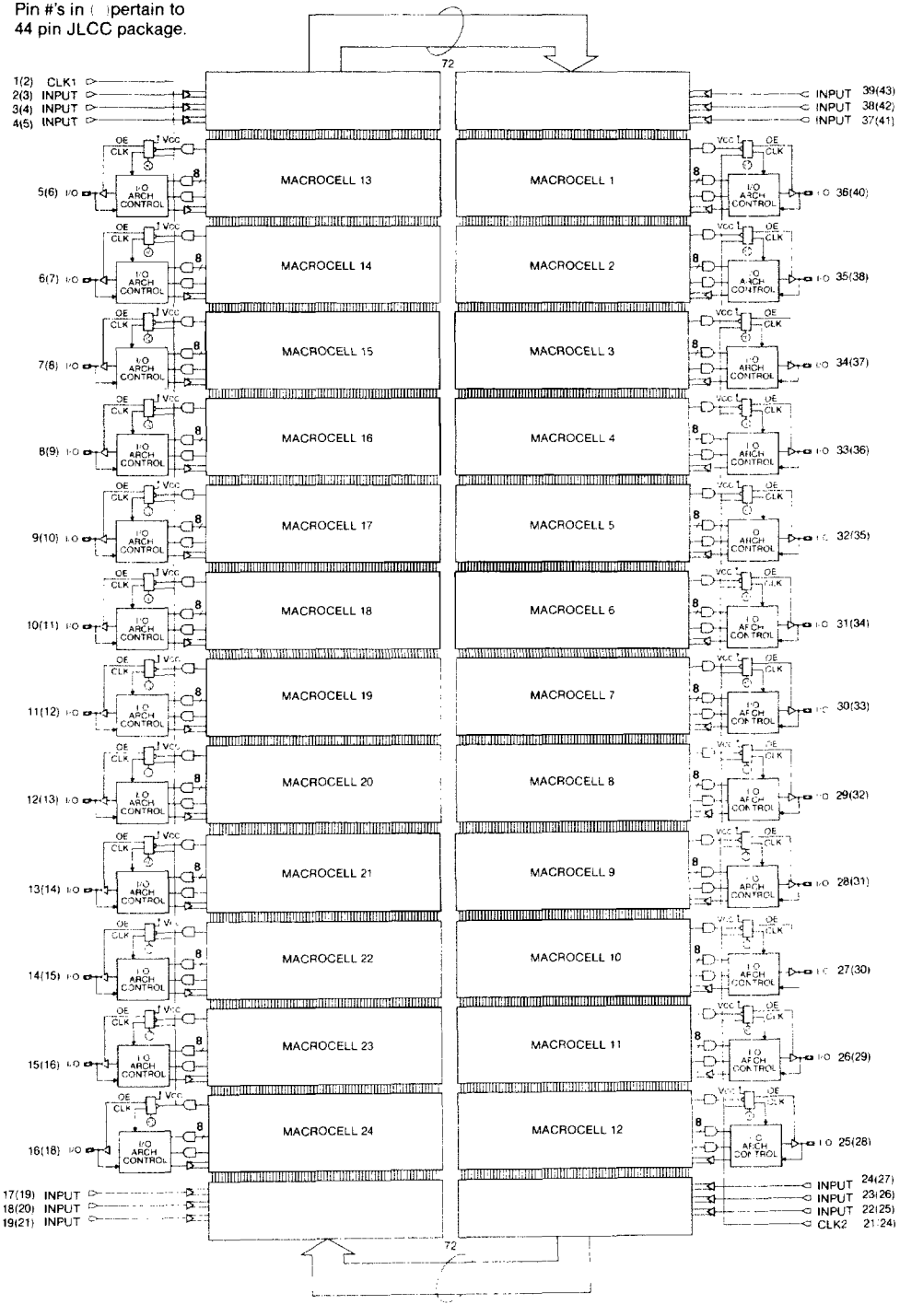
At the intersection point between an AND array input and a product term is an EPROM control cell. In the erased state, all cell connections are made. This means both the true and complement of all array inputs are connected to each product term. During the programming process, selected connections are opened. Therefore, any product term may be connected to the true or complement of any array input signal. When both the true and complement of an array input signal are left connected, a logical false results on the output of the AND gate. If both the true and complement of any array input signal are programmed open, then a logical "don't care" results for that input. If all 72 inputs for a given product term are programmed open, then a logical true results on the output of the corresponding AND gate. Two dedicated clock inputs (these two clock signals are not available in the AND array) provide the clock signals used for synchronous clocking of the EP900 internal registers. Each of these two clock signals is positive edge triggered and has control over a bank of 12 registers. "CLK1" controls Macrocells 13-24, while "CLK2" controls Macrocells 1-12. The EP900 advanced I/O architecture allows any number of the 24 internal registers to be user-defined for synchronous or asynchronous clock modes.

FIG. 1 LOGIC ARRAY MACROCELL



*Note ⊠ = I/O Pin, in which Logic Array input is from feedback path.
Pin numbers reflect 40 pin DIP.

FIG. 2 EP900 BLOCK DIAGRAM



I/O ARCHITECTURE

The EP900 Input/Output Architecture provides each Macrocell with over 50 programmable I/O configurations. Each I/O can be configured for combinatorial or registered output, with programmable output polarity. Four different register types (D, T, JK, SR) may be implemented into every I/O without additional logic requirements. I/O feedback selection can also be programmed for registered or input (from the pin) feedback. Another characteristic of the EP900 I/O architecture is the ability to individually clock each internal register from asynchronous clock signals.

OE/CLK Selection

Figure 3 shows the two modes of operation which are provided by the OE/CLK Select Multiplexer. The operation of this multiplexer is controlled by a single EPROM control bit and may be individually configured at each of the 24 I/O pins. In Mode 0, the three-state output buffer is controlled by the OE/CLK product term. (Recall that a single product term is equivalent to a 72 input AND gate.) If the output of the AND gate is a logical true, then the output buffer is enabled. If a logical false resides on the output of the AND gate, then the output buffer is seen as a high impedance node. In this mode the Macrocell flipflop is clocked by its respective synchronous clock input signal (CLK1 or CLK2). After erasure, the OE/CLK Select Mux is configured as Mode 0.

In Mode 1, the Output Enable buffer is tied to VCC (output is always enabled). The Macrocell flipflop may now be triggered from an asynchronous clock signal generated by the OE/CLK product term. This mode allows for individual clocking of flipflops from any of the 72 available AND array input signals. With both true and complement signals in the AND array, the flipflop may be configured to trigger on a rising or falling edge. In addition, this product term controlled clock configuration allows for the implementation of gated clock structures.

Figure 4 shows the basic output configurations available in the EP900. Along with combinatorial output, four register types are available. Each Macrocell may be individually configured. All registers have an individual Asynchronous Clear function which is controlled by a dedicated product term. When this product term yields a logical "1," the Macrocell register will immediately be loaded with a logical "0" independently of the clock. Upon power up of the EP900, the Clear function is performed automatically.

In the Combinatorial configuration, eight product terms are ORed together to acquire the output signal. The Invert Select EPROM bit controls output polarity and the Output Enable buffer is product term controlled. The Feedback Select Multiplexer allows the user to choose I/O (pin) feedback or no feedback to the AND array.

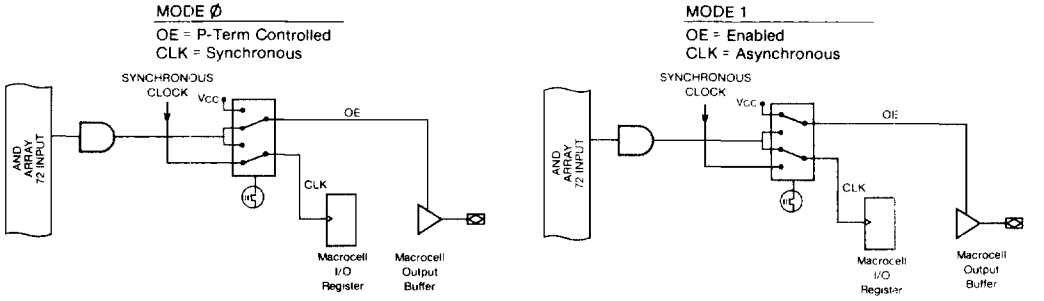
When the D or T register is selected, eight product terms are ORed together and made available to the register input. The Invert Select EPROM bit controls output polarity. The OE/CLK Select Multiplexer is used to configure the mode of operation (Mode 0 or Mode 1... see Figure 3). The Feedback Select Multiplexer allows the user to choose registered, I/O (pin) or no feedback to the AND array.

If the JK or SR register is selected, eight product terms are shared between two OR gates whose outputs feed the two primary register inputs. The allocation of product terms for each register input is optimized by the A+PLUS development software. The Invert Select EPROM bits control output polarity while the OE/CLK Select Multiplexer allows the mode of operation to be Mode 0 or Mode 1. The Feedback Select Multiplexer allows the user to choose registered or no feedback to the AND array.

Any I/O pin may be configured as a dedicated input by selecting no output with I/O (pin) feedback.

In the erased state, the I/O architecture is configured for combinatorial active low output with I/O (pin) feedback.

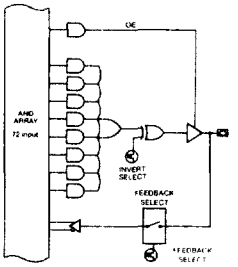
FIG. 3 OE/CLK SELECT MUX



The register is clocked by the synchronous clock signal which is common to 11 other Macrocells. The output is enabled by the logic from the product term.

The output is permanently enabled and the register is clocked via the product term. This allows for gated clocks that may be generated from elsewhere in the EP900.

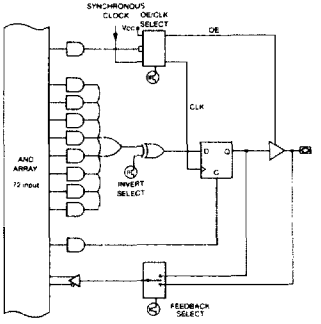
FIG. 4 I/O CONFIGURATIONS



COMBINATORIAL

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin



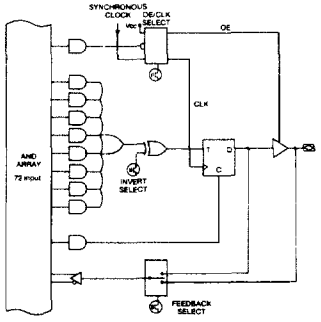
D-TYPE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
D-Register/High	D-Register, Pin, None
D-Register/Low	D-Register, Pin, None
None	D-Registered
None	Pin

FUNCTION TABLE

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1



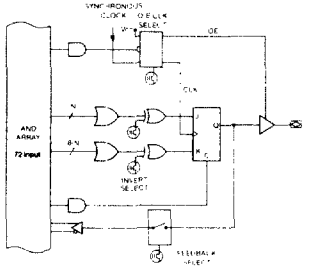
TOGGLE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T-Register / High	T-Register, Pin, None
T-Register / Low	T-Register, Pin, None
None	T-Register
None	Pin

FUNCTION TABLE

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0



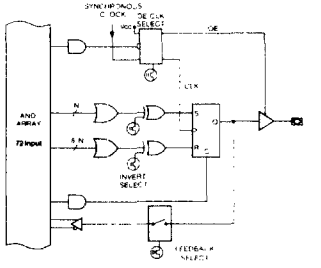
JK FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register

FUNCTION TABLE

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



SR FLIP-FLOP

I/O SELECTION

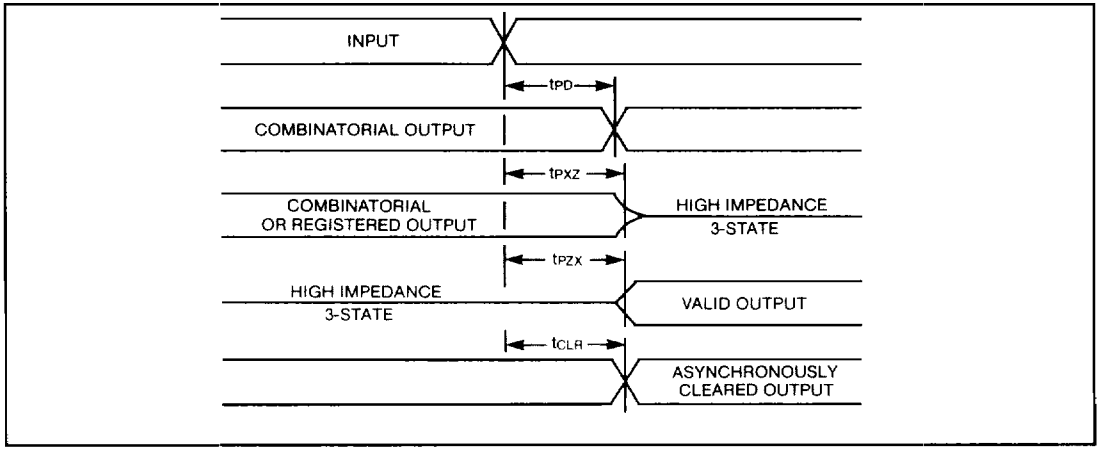
OUTPUT/POLARITY	FEEDBACK
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register

FUNCTION TABLE

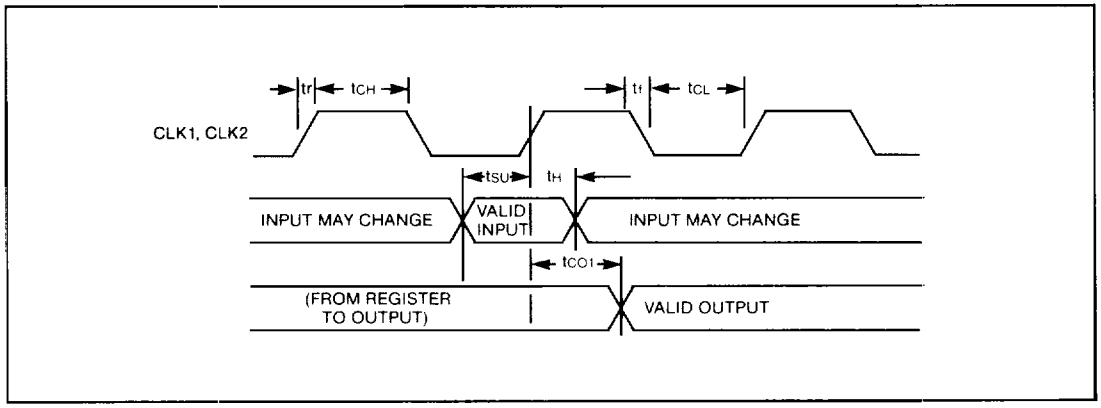
S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1

FIG. 5 SWITCHING WAVEFORMS

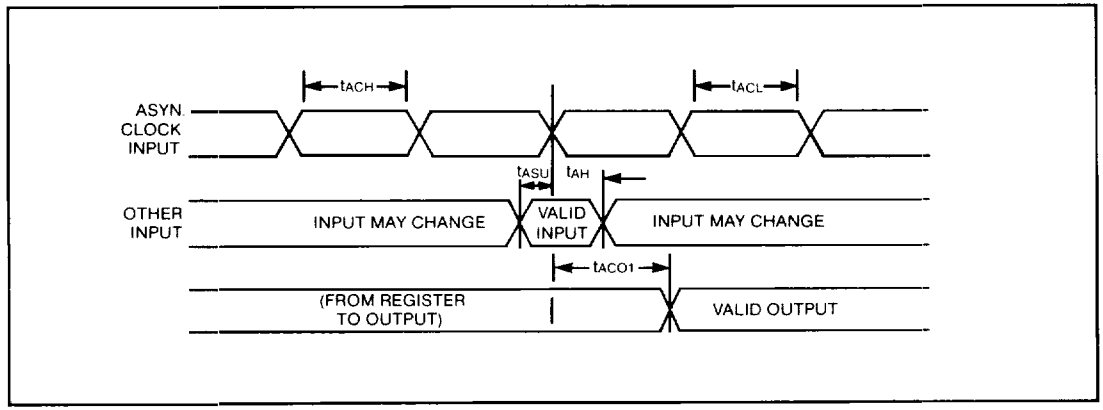
COMBINATORIAL MODE



SYNCHRONOUS CLOCK MODE



ASYNCHRONOUS CLOCK MODE



ABSOLUTE MAXIMUM RATINGS

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-150	+150	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			380	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias, note (6)	-65	+135	°C
ESD	ElectroStatic Discharge Voltage		±2100		V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage	note (6)	4.75 (4.5)	5.25 (5.5)	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_A	Operating temperature	For Industrial	-40	85	°C
T_A	Operating temperature	For Military	-55	125	°C
T_R	INPUT rise time	note (9)		500	ns
T_F	INPUT fall time	note (9)		500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ±10%, T_A = -55°C to 125°C for Military)
Note (1) and (6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND note (6)	-10 (-20)		+10 (+20)	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND note (6)	-10 (-20)		+10 (+20)	μA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load note (8)		10	150	μA
I_{CC2}	V_{CC} supply current (active)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		5	15 (25)	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		20	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF

AC CHARACTERISTICS Note (5)

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_A = -55°C to 125°C for Military)

			EP900-1		EP900-2		EP900-3		EP900		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t_{PD}	Input to non-registered output	C_1 = 50pF		35		45		50		60	ns
t_{PZX}	Input to output enable			35		45		50		60	ns
t_{PXZ}	Input to output disable	C_1 = 5pF note (2)		35		45		50		60	ns
t_{CLR}	Asynchronous output clear time	C_1 = 50pF		40		50		55		65	ns
t_{IO}	I/O input buffer delay			5		5		5		5	ns

SYNCHRONOUS CLOCK MODE

			EP900-1		EP900-2		EP900-3		EP900		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f_{MAX}	Maximum frequency		33.3		26.3		23.8		20		MHz
t_{SU}	Input setup time		30		38		42		50		ns
t_H	Input hold time		0		0		0		0		ns
t_{CH}	Clock high time		15		17.5		20		25		ns
t_{CL}	Clock low time		15		17.5		20		25		ns
t_{CO1}	Clock to output delay			22		25		27		30	ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal path)	note (7)		45		55		60		70	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (7)	22.2		18.2		16.7		14.3		MHz

ASYNCHRONOUS CLOCK MODE

			EP900-1		EP900-2		EP900-3		EP900		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f_{MAX}	Maximum frequency		33.3		26.3		23.8		20		MHz
t_{ASU}	Input setup time		12		13		14		15		ns
t_{AH}	Input hold time		15		15		15		15		ns
t_{ACH}	Clock high time		15		17.5		20		25		ns
t_{ACL}	Clock low time		15		17.5		20		25		ns
t_{ACO1}	Clock to output delay			40		50		55		65	ns
t_{ACNT}	Minimum clock period (register output feedback to register input - internal path)			45		55		60		70	ns
f_{ACNT}	Internal maximum frequency ($1/t_{ACNT}$)		22.2		18.2		16.7		14.3		MHz

Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Clock pin capacitance for dedicated clock inputs only. Pin 21, (high voltage pin during programming), has capacitance of 80 pF max.
5. All AC values tested with TURBO-BIT™ programmed.
6. Figures in ( ) pertain to military and industrial temperature versions.
7. Measured with device programmed as a 24 bit counter.
8. EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100 ns after last transition).
9. Clock t_R, t_F = 250ns (100ns).
10. The f_{MAX} values shown represent the highest frequency for pipelined data.

GRADE	AVAILABILITY	
Commercial (0°C to 70°C)	EP900-1	EP900-2
	EP900-3	EP900
Industrial (-40°C to 85°C)	EP900-3	EP900
Military (-55°C to 125°C)	EP900	

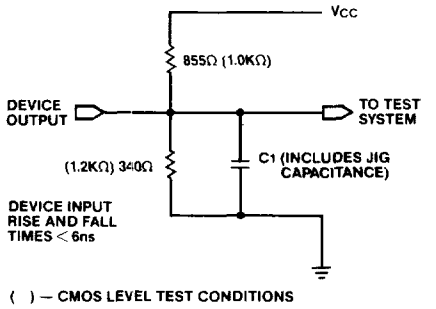
For devices other than those shown please consult factory.

FUNCTIONAL TESTING

The EP900 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP900 allows test programming patterns to be used and then erased. This facility to use application-independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices.

FIG. 6 AC TEST CONDITIONS



( ) — CMOS LEVEL TEST CONDITIONS

Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

DESIGN SECURITY

The EP900 contains a programmable design security feature that controls access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied nor retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

FIG. 7 I_{CC} VS F_{MAX}

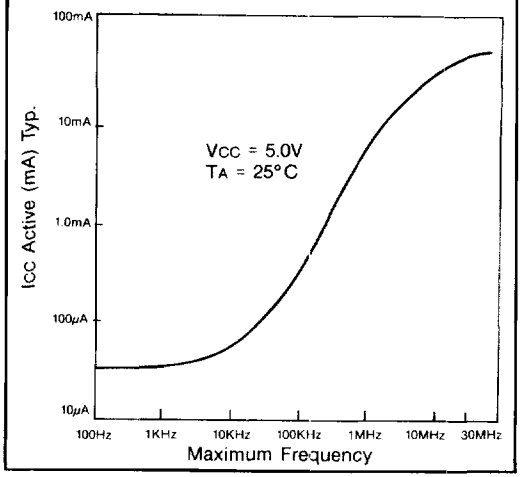


FIG. 8 OUTPUT DRIVE CURRENTS