EP610 EPLDs

High-Performance 16-Macrocell Devices

September 1991, ver. 2 **Data Sheet**

Features

- High-density replacement for TTL and 74HC with up to 600 gates
- High-performance 16-macrocell EPLD with t_{PD} = 15 ns and counter frequencies up to 83 MHz
- Zero-power operation (20 µA standby)
- Advanced CMOS EPROM technology to allow device erasure and reprogramming
- Individual clocking of all registers, or banked register operation from two global Clock inputs
- 16 macrocells with configurable I/O architecture, allowing up to 20 inputs and 16 outputs
- Programmable registers providing D, T, SR, or JK flip-flops with individual asynchronous Clear control
- 100% generically testable to provide 100% programming yield
- Programmable Security Bit for total protection of proprietary designs
- Available in 24-pin, 300-mil SOIC; 24-pin, 300-mil DIP; or 28-pin J-lead chip carriers
- Extensive third-party software and programming support

General Description

Altera's EP610 Erasable Programmable Logic Devices (EPLDs) can implement up to 600 equivalent gates of SSI and MSI logic functions in space-saving windowed ceramic or one-time-programmable (OTP) plastic 24-pin, 300-mil dual in-line package (CerDIP and PDIP) and 28-pin J-lead (JLCC and PLCC) packages, or OTP plastic 24-pin, 300-mil small-outline integrated circuit (SOIC) packages.

The EP610 EPLDs use sum-of-products logic that provides a programmable-AND/fixed-OR structure. These EPLDs accommodate combinatorial and sequential logic functions with up to 20 inputs and 16 outputs. The EP610 EPLDs also offer 60% more logic and 6 more flip-flops than a CMOS 22V10 device.

Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in active-high and active-low modes.

EP610 EPLDs can individually program D, T, SR, or JK flip-flop operation for each output without sacrificing product terms. In addition, each register can be individually clocked from any of the input or feedback paths in the AND array. These features make it possible to simultaneously implement a variety of logic functions.

The CMOS EPROM technology in the EP610 EPLDs can reduce active power consumption to less than 40% of the power required by equivalent bipolar devices, without losing speed. This reduced power consumption makes the EP610 EPLDs highly desirable for a wide range of applications. Moreover, these devices are 100% generically testable and can be erased with UV light. Designs and design modifications can be implemented quickly, eliminating the need for post-programming testing.

Logic is implemented with Altera's MAX+PLUS II or A+PLUS development systems. Both systems support schematic capture, Boolean equation, state machine, truth table, and netlist design entry methods. MAX+PLUS II also provides the Altera Hardware Description Language (AHDL), waveform entry, and EDIF 2 0 0 netlist interface. After the design is entered, the software automatically translates the input files into logic equations, performs Boolean minimization, and fits the design into the EPLD. MAX+PLUS II automatically partitions larger designs into multiple EPLDs. The device(s) can then be programmed in seconds at the designer's desktop to create customized working silicon. In addition, extensive third-party support exists for design entry, design processing, and device programming.

EP610 EPLDs

The EP610 EPLD is pin-, function-, and JEDEC-File-compatible with the EP610A, EP610T, and EP630 EPLDs. JEDEC Files generated for an EP610 EPLD can be used for programming these devices.

EP610

The EP610 EPLD combines high speed with low power. It can implement a 16-bit counter at up to 83.3 MHz, and typically consumes 5 mA when operating at 1 MHz. The EP610 EPLD is available with maximum t_{PD} values of 15, 20, 25, 30, and 35 ns. Both MIL-STD-883B-compliant and DESC-approved parts are available.

EP610A

The EP610A EPLD is a high-speed version of the EP610 device. It has a maximum t_{PD} of 10 ns, which is ideal for high-speed address decoding. The EP610A EPLD offers a 36% faster clock-to-output delay (t_{CO} = 6 ns) than a CMOS 22V10 and can easily integrate logic operating at today's faster system speeds. The EP610A EPLD is fabricated on an advanced 0.8-micron process, and supports 16-bit counter frequencies of up to 100 MHz.

EP610T

The EP610T EPLD is a lower-cost version of the EP610 device. This device operates in Turbo mode only. The Turbo Bit in the EPLD is preset at the factory. The EP610T EPLD is available with maximum t_{PD} values of 15 ns, 20 ns, and 25 ns.

EP630

T-90-01

The EP630 EPLD combines speed with a low-power standby mode. This device can implement a 16-bit counter at up to 83 MHz, and typically consumes 5 mA when operating at 1 MHz. It is available with maximum t_{PD} values of 15 ns and 20 ns.

Functional Description

The EP610 EPLDs use CMOS EPROM technology to configure connections in a programmable-AND logic array. EPROM connections are also used to construct a highly flexible programmable I/O architecture that provides advanced functions for user-programmable logic.

EP610 EPLDs have 4 dedicated data inputs, 2 global clock inputs, and 16 I/O pins that can be configured for input, output, or bidirectional operation on a macrocell-by-macrocell basis.

Each EP610 macrocell (see Figure 1) contains 10 product terms for the following functions: 8 product terms are dedicated to logic implementation; 1 product term is used for Clear control of the internal register; and 1 product term implements either Output Enable or an array Clock.

Figure 1. EP610 Macrocell

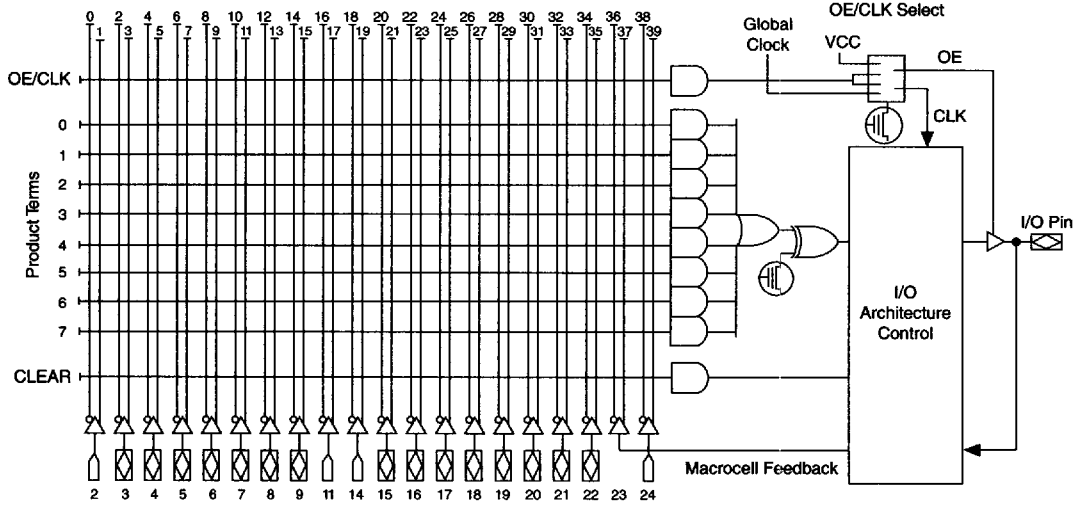
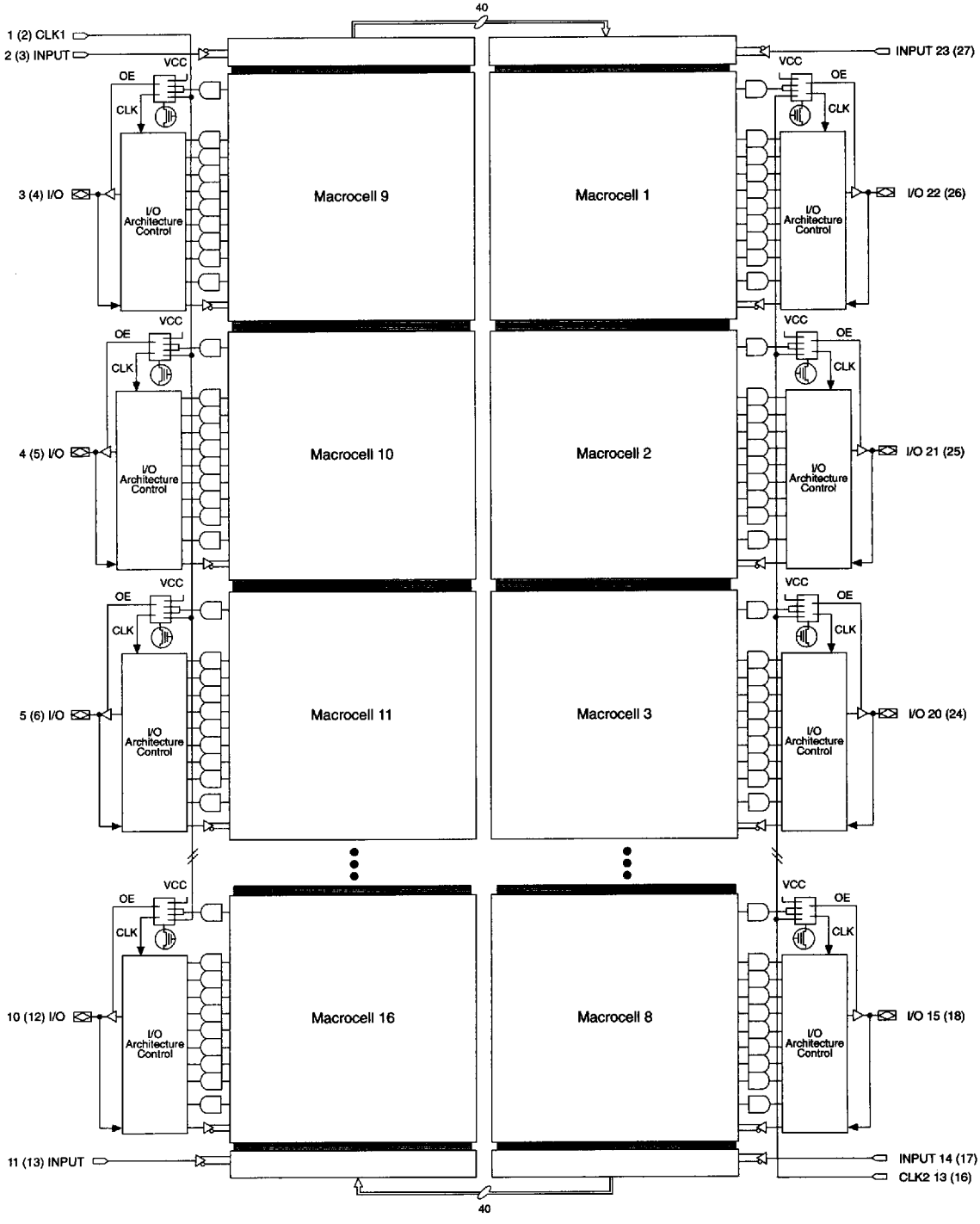


Figure 2 shows the complete block diagram of an EP610 EPLD. The internal device architecture has a sum-of-products (AND/OR) structure. Inputs to the programmable-AND array come from the true and complement signals of the 4 dedicated data inputs and 16 I/O feedback signals. The 40-input AND array has 160 product terms distributed among the 16 macrocells. Each product term represents a 40-input AND gate.

Figure 2. EP610 Block Diagram *Numbers in parentheses are for J-lead packages.* T-90-01



In the erased state, the true and complement of the AND-array inputs are connected to the product terms. An EPROM control cell is located at each intersection of an AND-array input and a product term. During programming, selected connections are opened, allowing any product term to be connected to a true or complement array input signal with the following results:

- If both the true and complement of an array input signal are connected, the output of the AND gate is a logic low.
- If both the true and complement of any array input signal are programmed "open," a logic "don't care" results for that input.
- If all inputs for a given product term are programmed "open," the output of the corresponding AND gate is a logic high.

Two dedicated Clock inputs (which are not available in the AND array) provide the signals used for global clocking of EP610 internal registers. Each signal is positive-edge-triggered and has control over 8 registers: CLK1 controls macrocells 9 to 16; CLK2 controls macrocells 1 to 8. The programmable I/O architecture allows each of the 16 internal registers to have a global or array (product-term) Clock.

I/O Architecture

The EP610 architecture provides each macrocell with over 50 programmable I/O configurations. Each macrocell can be configured for combinatorial or registered output, with programmable output polarity. One of four register types (D, T, JK, and SR) can be implemented in each macrocell without additional logic. I/O feedback selection can be programmed for registered or input feedback. The I/O architecture can also individually clock each internal register from any internal signal.

OE/CLK Selection

Figure 3 shows the two modes of operation provided by the OE/CLK Select multiplexer. This multiplexer, which is controlled by a single EPROM bit, can be individually configured at each I/O pin.

In Mode 0, the tri-state output buffer is controlled by a single product term. If the output of the AND gate is high, then the output buffer is enabled. If the output is low, the output buffer has a high-impedance value. In this mode, the macrocell flip-flop is clocked by its global Clock input signal (CLK1 or CLK2). In the erased state, the OE/CLK Select multiplexer is configured to Mode 0.

In Mode 1, the Output Enable buffer is always enabled, allowing the macrocell flip-flop to be triggered from an array Clock signal generated by the OE/CLK product term. This mode allows flip-flops to be individually clocked from any of the AND-array input signals. With true and complement signals in the AND array, the flip-flop can be configured to trigger on a rising or falling edge. This product-term-controlled clock configuration also allows implementation of gated clock structures.

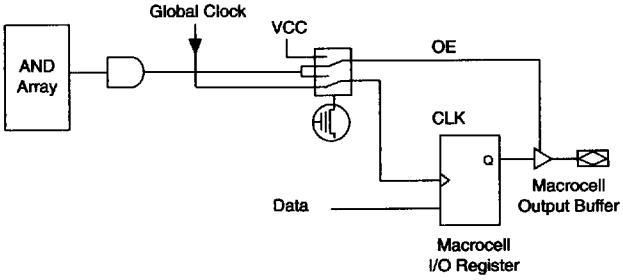
T-90-01

Figure 3. OE/CLK Select Multiplexer

Mode 0:

The register is clocked by the global Clock signal, which can be connected to seven other macrocells. The output is enabled by the logic from the product term.

OE = Array (Product Term)
CLK = Global



Mode 1:

The output is permanently enabled and the register is clocked by the product term, which allows gated clocks to be generated in EP610 EPLDs.

OE = Enabled
CLK = Array

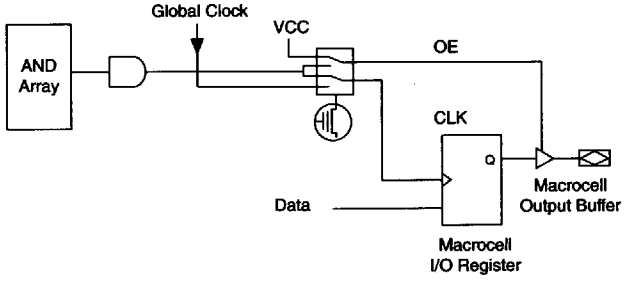
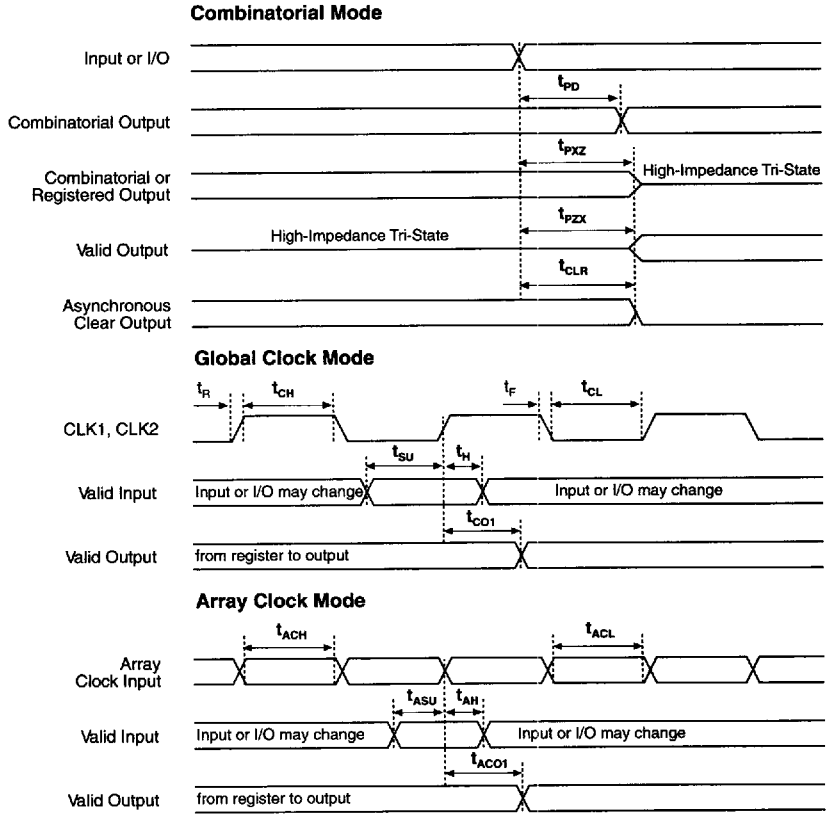


Figure 4 shows waveforms for the following modes: combinatorial, global Clock, and array Clock.

T-90-01

Figure 4. EP610 Switching Waveforms

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

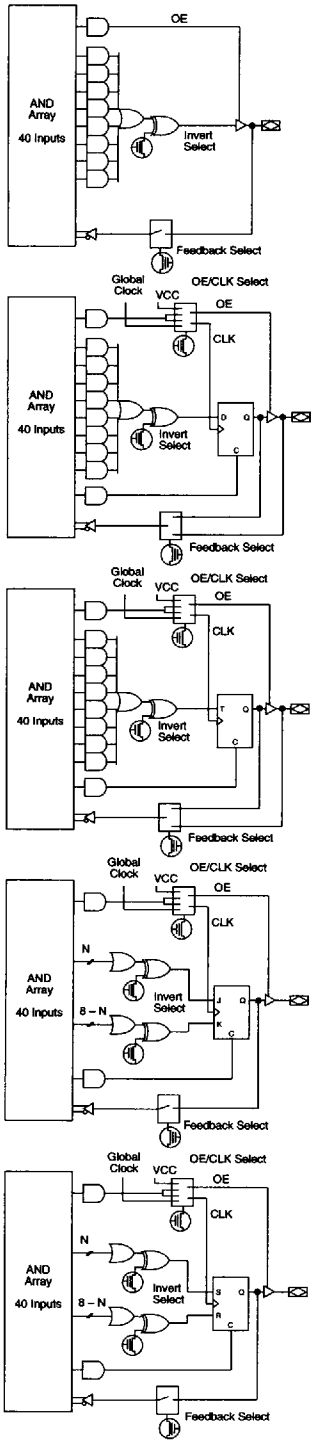


Output/ Feedback Selection

Output configurations available with the EP610 EPLDs are shown in Figure 5. Each macrocell can be individually configured with combinatorial output or with any of the four register outputs. All registers have an individual asynchronous Clear function controlled by a dedicated product term. When this product term is a logic high, the macrocell register is immediately loaded with a logic low. The Clear function is performed automatically during power-up.

T-90-01

Figure 5. EP610 I/O Configurations



Combinatorial

I/O Selection

Output/Polarity	Feedback
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin

D Flip-Flop

I/O Selection

Output/Polarity	Feedback
D Register/High	D Register, Pin, None
D Register/Low	D Register, Pin, None
None	D Register
None	Pin

Function Table

D	Q_n	Q_{n+1}
L	L	L
L	H	L
H	L	H
H	H	H

T Flip-Flop

I/O Selection

Output/Polarity	Feedback
T Register/High	T Register, Pin, None
T Register/Low	T Register, Pin, None
None	T-Register
None	Pin

Function Table

T	Q_n	Q_{n+1}
L	L	L
L	H	H
H	L	H
H	H	L

JK Flip-Flop

I/O Selection

Output/Polarity	Feedback
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register

Function Table

J	K	Q_n	Q_{n+1}
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

SR Flip-Flop

I/O Selection

Output/Polarity	Feedback
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register

Function Table

S	R	Q_n	Q_{n+1}
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	H

The combinatorial configuration has eight product terms ORed together to generate the output signal. This configuration has the following characteristics:

- The Invert Select EPROM bit controls output polarity.
- One product term controls the Output Enable buffer.
- The Feedback-Select multiplexer allows the user to choose I/O (pin) feedback or no feedback to the AND array.

The D or T register has eight product terms ORed together that are available to the register input. This configuration has the following characteristics:

- The Invert Select EPROM bit controls output polarity.
- One product term controls asynchronous Clear.
- The OE/CLK Select multiplexer configures the mode of operation to Mode 0 or Mode 1.
- The Feedback Select multiplexer allows the user to choose registered feedback, I/O feedback, or no feedback to the AND array.

If the JK or SR register is selected, eight product terms are shared between two OR gates. The outputs of the OR gates feed the two primary register inputs. This configuration has the following characteristics:

- The MAX+PLUS II and A+PLUS development systems optimize the allocation of product terms for each register input.
- One product term controls asynchronous Clear.
- The Invert Select EPROM bits control output polarity.
- The OE/CLK Select multiplexer configures the mode of operation to Mode 0 or Mode 1.
- The Feedback Select multiplexer allows the user to choose registered feedback or no feedback to the AND array.

Any I/O pin can be configured as a dedicated input by selecting no output with I/O feedback. In the erased state, the I/O architecture is configured for combinatorial active-low output with I/O feedback.

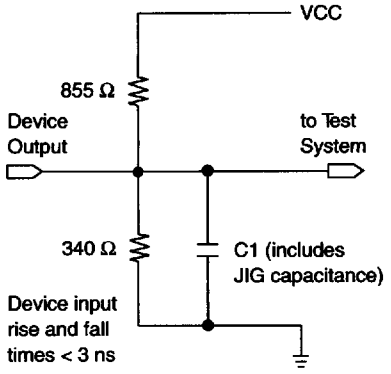
Functional Testing

EP610 EPLDs are fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements. A 100% programming yield is ensured. This testing process eliminates problems associated with fuse-programmed circuits by allowing test programming patterns to be used and then erased. The ability to use application-independent, general-purpose tests, called generic testing, is unique to EPLDs. AC test measurements are performed under the conditions shown in Figure 6.

T-90-01

Figure 6. EP610 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.



Design Security

The EP610 EPLDs contain a programmable design Security Bit that controls access to the data programmed into the device. If this feature is used, a proprietary design implemented in the EPLD cannot be copied or retrieved. This feature provides a high level of design security by making programmed data within EPROM cells invisible. The Security Bit, as well as all other program data, is reset by erasing the EPLD.

Turbo Bit

EP610 EPLDs contain a programmable Turbo Bit, set with the design software, to control the automatic power-down feature that enables the low-standby-power mode. When the Turbo Bit is programmed (Turbo = On), the low-standby-power mode (I_{CC1}) is disabled, making the circuit less sensitive to V_{CC} noise transients created by the low-power mode power-up/power-down cycle. All AC values are tested with the Turbo Bit programmed.

If the design requires low-power operation, the Turbo Bit should be disabled (Turbo = Off). In this mode, some AC parameters may increase. To determine worst-case timing, values from the AC Non-Turbo Adder specifications must be added to the corresponding AC parameter.

EP610 EPLD

T-46-19-09

Features

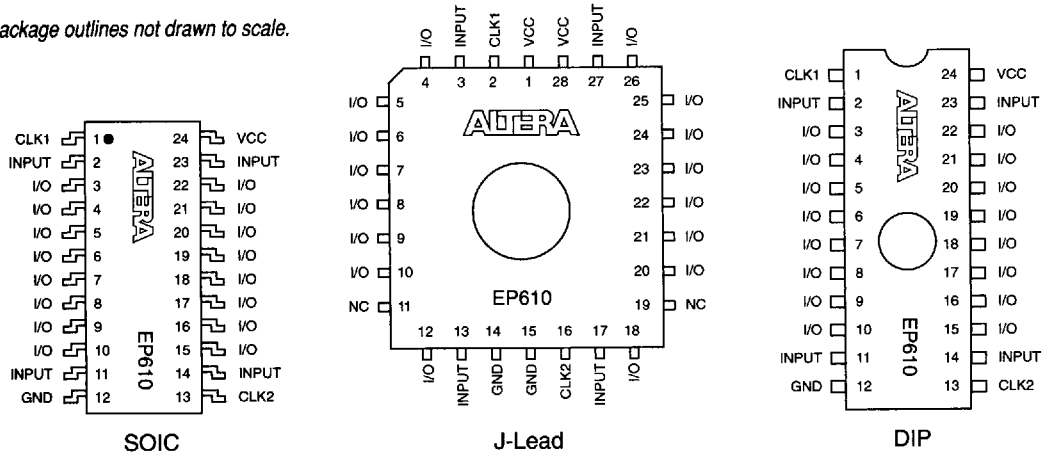
- Highest-performance 16-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 83 MHz
  - Pipelined data rates up to 83 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP610A, EP610T, and EP630 EPLDs
- 100% generically testable to provide 100% programming yield
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages:
  - 24-pin dual in-line package (CerDIP and PDIP)
  - 24-pin small-outline integrated circuit (plastic SOIC only)
  - 28-pin J-lead chip carrier (JLCC and PLCC)
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP610 Erasable Programmable Logic Device (EPLD) can implement up to 600 equivalent gates of SSI and MSI logic functions. It is available in space-saving windowed ceramic or OTP plastic 24-pin, 300-mil DIP and 28-pin J-lead packages, or OTP plastic 24-pin, 300-mil SOIC packages. See Figure 7.

Figure 7. EP610 Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	°C
T_A	Operating temperature	For industrial use	–40	85	°C
T_C	Case temperature	For military use	–55	125	°C
t_R	Input rise time	*See Note (3)*		100 (50)	ns
t_F	Input fall time	*See Note (3)*		100 (50)	ns

DC Operating Conditions

See Notes (2), (4), (5)

Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage			–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC		2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC		3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC				0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND		–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND		–10		10	µA
I_{CC1}	V_{CC} supply current (non-turbo standby)	V_I = V_{CC} or GND, No load, *See Note (6)*	-15, -20, -25, -30, -35		20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo mode)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *See Note (7)*	-15, -20		5	10	mA
			-25, -30, -35		5	10 (15)	mA
I_{CC3}	V_{CC} supply current (turbo mode)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *See Note (7)*	-15, -20		45	90	mA
			-25, -30, -35		45	60 (75)	mA

T-46-19-09

Capacitance *See Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions: EP610-15 and EP610-20 *See Note (5)*

			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (9)*	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	20	ns
t_{PD2}	I/O input to non-registered output			17		22	20	ns
t_{PZX}	Input to output enable			15		20	20	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (10)*		15		20	20	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20	20	ns
t_{IO}	I/O input pad and buffer delay			2		2	0	ns

Global Clock Mode			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (9)*	Unit
f_{MAX}	Maximum frequency	*See Note (11)*	83.3		62.5		0	MHz
t_{SU}	Input setup time		9		11		20	ns
t_{H}	Input hold time		0		0		0	ns
t_{CH}	Clock high time		6		8		0	ns
t_{CL}	Clock low time		6		8		0	ns
t_{CO1}	Clock to output delay			11		13	0	ns
t_{CNT}	Minimum clock period			12		16	0	ns
f_{CNT}	Internal maximum frequency	*See Note (7)*	83.3		62.5		0	MHz

Array Clock Mode			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (9)*	Unit
f_{MAX}	Maximum frequency	*See Note (11)*	71.4		55.5		0	MHz
t_{ASU}	Input setup time		6		8		20	ns
t_{AH}	Input hold time		6		8		0	ns
t_{ACH}	Clock high time		7		9		0	ns
t_{ACL}	Clock low time		7		9		0	ns
t_{ACO1}	Clock to output delay			15		20	20	ns
t_{ACNT}	Minimum clock period			14		18	0	ns
f_{ACNT}	Internal maximum frequency	*See Note (7)*	71.4		55.5		0	MHz

T-46-19-09

AC Operating Conditions: EP610-25, EP610-30, and EP610-35 *See Note (5)*

			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	30	ns
t_{PD2}	I/O input to non-registered output			27		32		37	30	ns
t_{PZX}	Input to output enable			25		30		35	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *See Note (10)*		25		30		35	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		27		32		37	30	ns
t_{IO}	I/O input pad and buffer delay			2		2		2	0	ns

Global Clock Mode			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*See Note (11)*	47.6		41.7		37.0		0	MHz
t_{SU}	Input setup time		21		24		27		30	ns
t_{H}	Input hold time		0		0		0		0	ns
t_{CH}	Clock high time		10		11		12		0	ns
t_{CL}	Clock low time		10		11		12		0	ns
t_{CO1}	Clock to output delay			15		17		20	0	ns
t_{CNT}	Minimum clock period			25		30		35	0	ns
f_{CNT}	Internal maximum frequency	*See Note (7)*	40.0		33.3		28.6		0	MHz

Array Clock Mode			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*See Note (11)*	47.6		41.7		37.0		0	MHz
t_{ASU}	Input setup time		8		8		8		30	ns
t_{AH}	Input hold time		12		12		12		0	ns
t_{ACH}	Clock high time		10		11		12		0	ns
t_{ACL}	Clock low time		10		11		12		0	ns
t_{ACO1}	Clock to output delay			27		32		37	30	ns
t_{ACNT}	Minimum clock period			25		30		35	0	ns
f_{ACNT}	Internal maximum frequency	*See Note (7)*	40.0		33.3		28.6		0	MHz

T-46-19-09

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP610-15 and EP610-20 EPLDs: maximum V_{PP} is 14.0 V.
(2) Numbers in parentheses are for military and industrial temperature versions.
(3) For EP610-15 and EP610-20 EPLDs: t_R and t_F = 40 ns. For EP610-15 and EP610-20 clocks: t_R and t_F = 20 ns.
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) When in non-turbo mode, an EPLD will automatically enter standby mode if logic transitions do not occur (approximately 100 ns after the last transition).
(7) Measured with a device programmed as a 16-bit counter.
(8) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. For EP610-25, EP610-30, and EP610-35 EPLDs: Pin 13 (high-voltage pin during programming) has a maximum capacitance of 50 pF; C_{IN}, C_{OUT}, and C_{CLK} = 20 pF.
(9) See "Turbo Bit" earlier in this data sheet.
(10) Sample-tested only for an output change of 500 mV.
(11) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

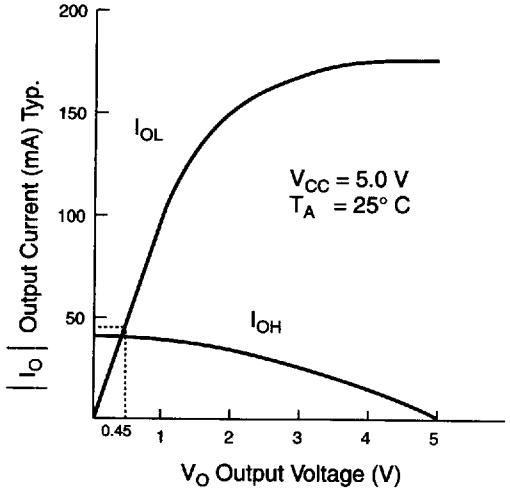
Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP610-15, EP610-20, EP610-25, EP610-30, EP610-35
Industrial	(–40° C to 85° C)	EP610-20, EP610-30, EP610-35
Military	(–55° C to 125° C)	EP610-35

Note: Only military-temperature-range devices are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera's Marketing Department at (408) 984-2800. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

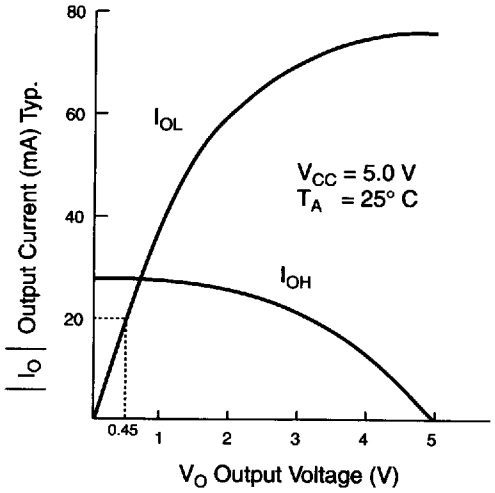
Figure 8 shows the output drive characteristics for EP610 I/O pins and typical supply current versus frequency for the EP610 EPLDs.

Figure 8. EP610 Output Drive Characteristics and I_{CC} vs. Frequency

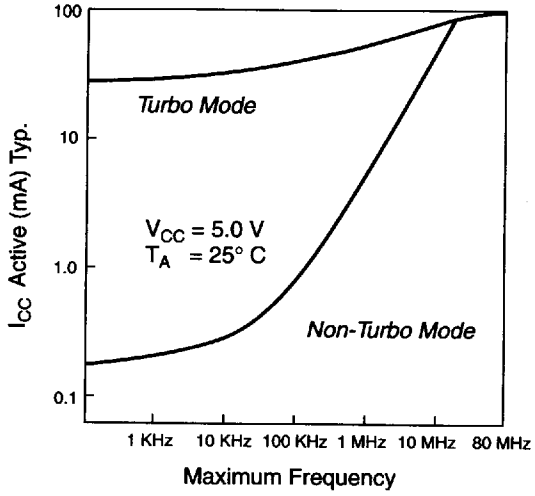
EP610-15 and EP610-20 EPLDs



EP610-25, EP610-30, and EP610-35 EPLDs



All EP610 EPLDs



EP610A EPLD

T-46-19-09

Features

- Highest-performance 16-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 10 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 100 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP610, EP610T, and EP630 EPLDs
- 100% generically testable to provide 100% programming yield
- Available in reprogrammable plastic chip carrier packages:
  - 24-pin dual in-line package (PDIP)
  - 24-pin small-outline integrated circuit (SOIC)
  - 28-pin J-lead chip carrier (PLCC)
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

Advance Information

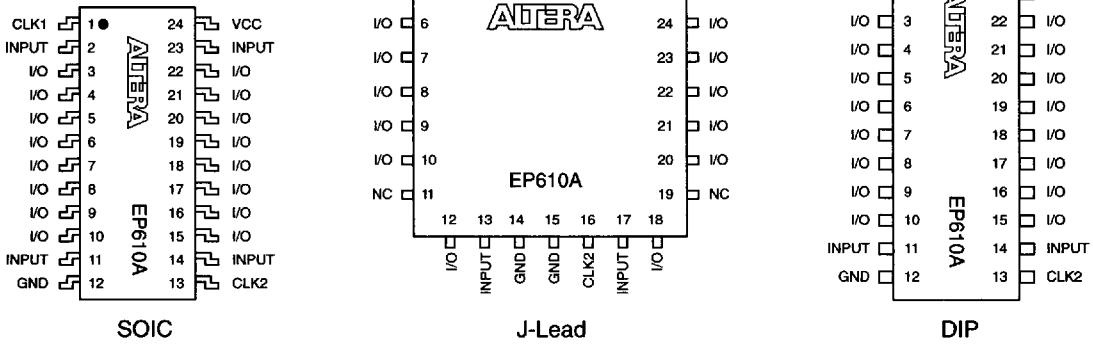
2 Classic EPLDs

General Description

Altera's EP610A Erasable Programmable Logic Device (EPLD) is a high-speed version of the EP610 EPLD. It offers enhanced performance and is available in reprogrammable plastic 24-pin, 300-mil DIP; 24-pin SOIC; and 28-pin J-lead chip carrier packages. It is also available with maximum t_{PD} values of 10 ns and 12 ns. See Figure 9.

Figure 9. EP610A Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			25	ns
t_F	Input fall time			25	ns

DC Operating Conditions

See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.5	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		45	90	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (4)*		45	90	mA

Capacitance

See Note (5)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		16	pF

T-46-19-09

AC Operating Conditions *See Note (3)*

			EP610A-10		EP610A-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		10		12	ns
t_{PD2}	I/O input to non-registered output			10		12	ns
t_{PZX}	Input to output enable			10		12	ns
t_{PXZ}	Input to output disable, *See Note (6)*	C1 = 5 pF		10		12	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		10		12	ns

Global Clock Mode			EP610A-10		EP610A-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*See Note (7)*	100		83.3		MHz
t_{SU}	Input setup time		8		8		ns
t_{H}	Input hold time		0		0		ns
t_{CH}	Clock high time		5		6		ns
t_{CL}	Clock low time		5		6		ns
t_{CO1}	Clock to output delay			6		6	ns
t_{CNT}	Minimum clock period			10		12	ns
f_{CNT}	Internal maximum frequency	*See Note (4)*	100		83.3		MHz

Array Clock Mode			EP610A-10		EP610A-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*See Note (7)*	100		83.3		MHz
t_{ASU}	Input setup time		5		6		ns
t_{AH}	Input hold time		5		6		ns
t_{ACH}	Clock high time		5		6		ns
t_{ACL}	Clock low time		5		6		ns
t_{ACO1}	Clock to output delay			12		13	ns
t_{ACNT}	Minimum clock period			10		12	ns
f_{ACNT}	Internal maximum frequency	*See Note (4)*	100		83.3		MHz

T-46-19-09

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(3) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a device programmed as a 16-bit counter.
(5) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. Pin 13 (high-voltage pin during programming) has a maximum capacitance of 50 pF.
(6) Sample-tested only for an output change of 500 mV.
(7) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	Consult factory
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

EP610T EPLD

T-46-19-09

Features

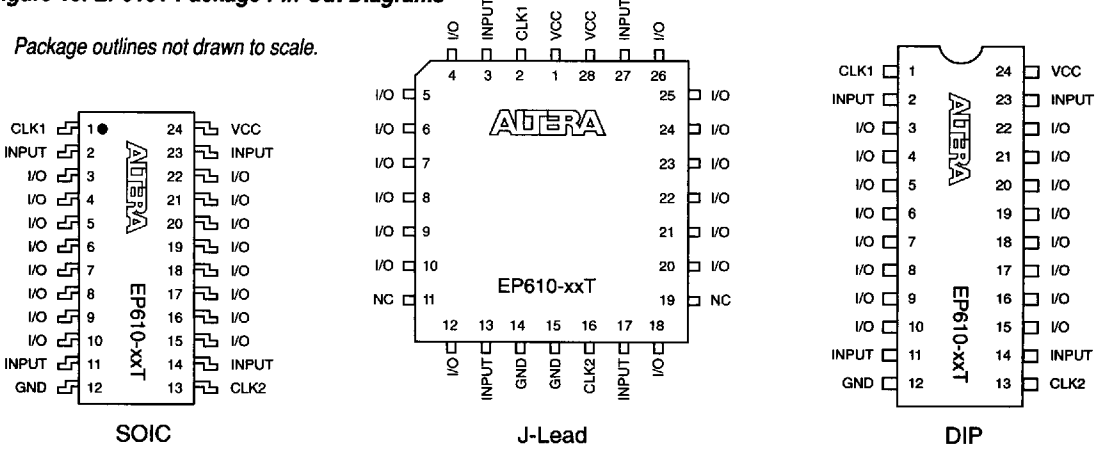
- High-performance 16-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 83 MHz
  - Pipelined data rates up to 83 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP610, EP610A, and EP630 EPLDs
- 100% generically testable to provide 100% programming yield
- Available in low-cost one-time-programmable (OTP) plastic chip carrier packages
  - 24-pin, 300-mil dual in-line package (PDIP)
  - 24-pin small-outline integrated circuit (SOIC)
  - 28-pin J-lead chip carrier (PLCC)
- Programmable clock option allowing independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP610T Erasable Programmable Logic Device (EPLD) is a low-cost, high-performance version of the EP610 device. This EPLD operates in a turbo mode that is optimized for high-speed applications. The Turbo Bit in the device is preset at the factory. The EP610T EPLD is available in OTP plastic 24-pin, 300-mil DIP; 24-pin SOIC; and 28-pin J-lead chip carrier packages with maximum t_{PD} values of 15 ns, 20 ns, and 25 ns. See Figure 10.

Figure 10. EP610T Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time	*See Note (2)*		100	ns
t_F	Input fall time	*See Note (2)*		100	ns

DC Operating Conditions *See Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		60	90	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		60	90	mA

Capacitance *See Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

T-46-19-09

AC Operating Conditions *See Note (4)*

Symbol	Parameter	Conditions	EP610-15T Min	EP610-15T Max	EP610-20T Min	EP610-20T Max	EP610-25T Min	EP610-25T Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20		25	ns
t_{PD2}	I/O input to non-registered output			17		22		27	ns
t_{PZX}	Input to output enable			15		20		25	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *See Note (7)*		15		20		25	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20		27	ns
t_{IO}	I/O input pad and buffer delay			2		2		2	ns

Global Clock Mode Symbol	Parameter	Conditions	EP610-15T Min	EP610-15T Max	EP610-20T Min	EP610-20T Max	EP610-25T Min	EP610-25T Max	Unit
f_{MAX}	Maximum frequency	*See Note (8)*	83.3		62.5		47.6		MHz
t_{SU}	Input setup time		9		11		21		ns
t_{H}	Input hold time		0		0		0		ns
t_{CH}	Clock high time		6		8		10		ns
t_{CL}	Clock low time		6		8		10		ns
t_{CO1}	Clock to output delay			11		13		15	ns
t_{CNT}	Minimum clock period			12		16		25	ns
f_{CNT}	Internal maximum frequency	*See Note (5)*	83.3		62.5		40.0		MHz

Array Clock Mode Symbol	Parameter	Conditions	EP610-15T Min	EP610-15T Max	EP610-20T Min	EP610-20T Max	EP610-25T Min	EP610-25T Max	Unit
f_{MAX}	Maximum frequency	*See Note (8)*	71.4		55.5		47.6		MHz
t_{ASU}	Input setup time		6		8		8		ns
t_{AH}	Input hold time		6		8		12		ns
t_{ACH}	Clock high time		7		9		10		ns
t_{ACL}	Clock low time		7		9		10		ns
t_{ACO1}	Clock to output delay			15		20		27	ns
t_{ACNT}	Minimum clock period			14		18		25	ns
f_{ACNT}	Internal maximum frequency	*See Note (5)*	71.4		55.5		40.0		MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP610-15T and EP610-20T: Maximum V_{PP} is 14.0V.
(2) For EP610-15T and EP610-20T EPLDs: t_R and t_F = 40 ns. For EP610-15T and EP610-20T clocks: t_R and t_F = 20 ns.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
(5) Measured with a device programmed as a 16-bit counter.
(6) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. For EP610-25T: Pin 13 (high-voltage pin during programming) has a maximum capacitance of 50 pF; C_{IN}, C_{OUT}, and C_{CLK} = 20 pF.
(7) Sample-tested only for an output change of 500 mV.
(8) The f_{MAX} values represent the highest frequency for pipelined data.

T-46-19-09

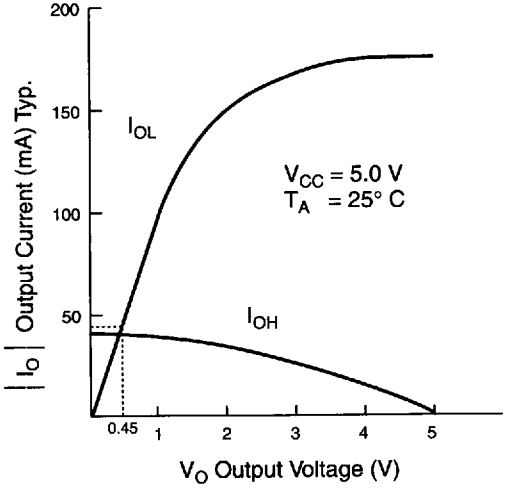
Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP610-15T, EP610-20T, EP610-25T
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

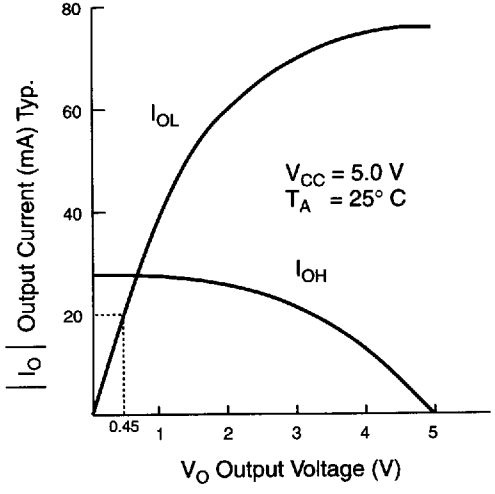
Figure 11 shows the output drive characteristics for EP610T I/O pins and typical supply current versus frequency for the EP610T EPLD.

Figure 11. EP610T Output Drive Characteristics and I_{CC} vs. Frequency

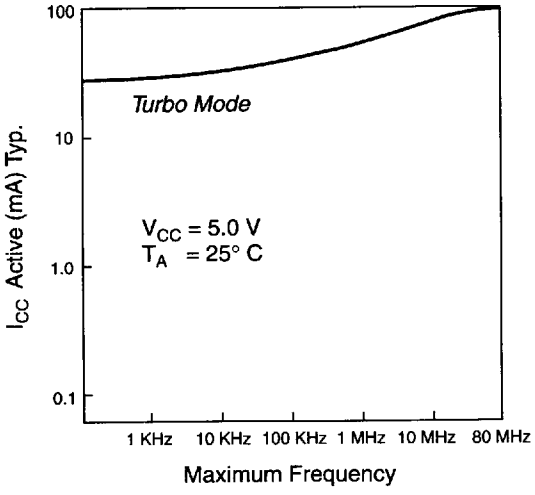
EP610-15T and EP610-20T EPLDs



EP610-25T EPLD



All EP610T EPLDs



EP630 EPLD

T-46-19-09

Features

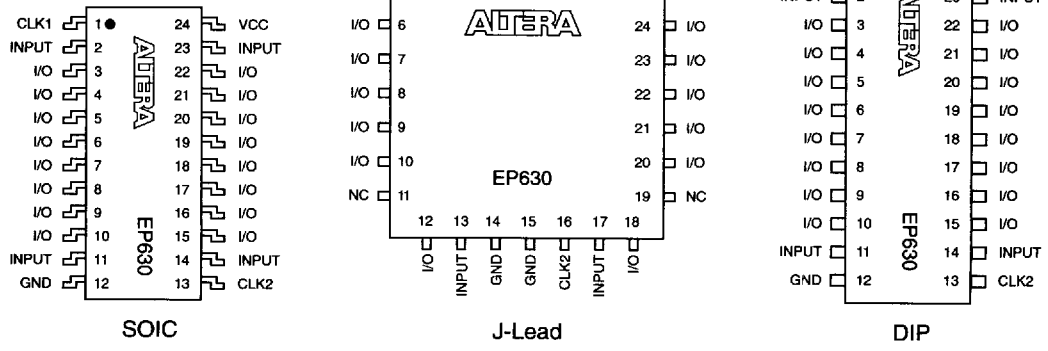
- High-performance 16-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 83 MHz
  - Pipelined data rates up to 83 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP610, EP610A, and EP610T EPLDs
- 100% generically testable to provide 100% programming yield
- Available in one-time-programmable (OTP) plastic chip carrier packages
  - 24-pin, 300-mil dual in-line package (PDIP)
  - 24-pin, 300-mil small-outline integrated circuit (SOIC)
  - 28-pin J-lead chip carrier (PLCC)
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP630 Erasable Programmable Logic Device (EPLD) is a fast, low-power version of the EP610 device. The EP630 EPLD can implement a 16-bit counter at up to 83 MHz and typically consumes 5 mA when operating at 1 MHz. The EP630 EPLD is available in OTP plastic 24-pin, 300-mil DIP; 24-pin, 300-mil SOIC; and 28-pin J-lead chip carrier packages. It is available with maximum t_{PD} values of 15 ns and 20 ns. See Figure 12.

Figure 12. EP630 Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	14.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time	*See Note (2)*		40	ns
t_F	Input fall time	*See Note (2)*		40	ns

DC Operating Conditions

See Notes (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (non-turbo standby)	$V_I = V_{CC}$ or GND, No load, *See Note (5)*		20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (6)*		5	10	mA
I_{CC3}	V_{CC} supply current (turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (6)*		45	90	mA

T-46-19-09

Capacitance *See Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (4)*

			EP630-15		EP630-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (8)*	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	20	ns
t_{PD2}	I/O input to non-registered output			17		22	20	ns
t_{PZX}	Input to output enable			15		20	20	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (9)*		15		20	20	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20	20	ns
t_{IO}	I/O input pad and buffer delay			2		2	0	ns

Global Clock Mode			EP630-15		EP630-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (8)*	Unit
f_{MAX}	Maximum frequency	*See Note (10)*	83.3		62.5		0	MHz
t_{SU}	Input setup time		9		11		20	ns
t_{H}	Input hold time		0		0		0	ns
t_{CH}	Clock high time		6		8		0	ns
t_{CL}	Clock low time		6		8		0	ns
t_{CO1}	Clock to output delay			11		13	0	ns
t_{CNT}	Minimum clock period			12		16	0	ns
f_{CNT}	Internal maximum frequency	*See Note (6)*	83.3		62.5		0	MHz

Array Clock Mode			EP630-15		EP630-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (8)*	Unit
f_{MAX}	Maximum frequency	*See Note (10)*	71.4		55.5		0	MHz
t_{ASU}	Input setup time		6		8		20	ns
t_{AH}	Input hold time		6		8		0	ns
t_{ACH}	Clock high time		7		9		0	ns
t_{ACL}	Clock low time		7		9		0	ns
t_{ACO1}	Clock to output delay			15		20	20	ns
t_{ACNT}	Minimum clock period			14		18	0	ns
f_{ACNT}	Internal maximum frequency	*See Note (6)*	71.4		55.5		0	MHz

T-46-19-09

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) For all clocks: t_R and t_F = 20 ns.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(5) When in non-turbo mode, an EPLD will automatically enter standby mode if logic transitions do not occur (approximately 100 ns after the last transition).
(6) Measured with a device programmed as a 16-bit counter.
(7) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only.
(8) See "Turbo Bit" earlier in this data sheet.
(9) Sample-tested only for an output change of 500 mV.
(10) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP630-15, EP630-20
Industrial	(–40° C to 85° C)	EP630-20
Military	(–55° C to 125° C)	Consult factory

Figure 13 shows the output drive characteristics for EP630 I/O pins and typical supply current versus frequency for the EP630 EPLD.

Figure 13. EP630 Output Drive Characteristics and I_{CC} vs. Frequency