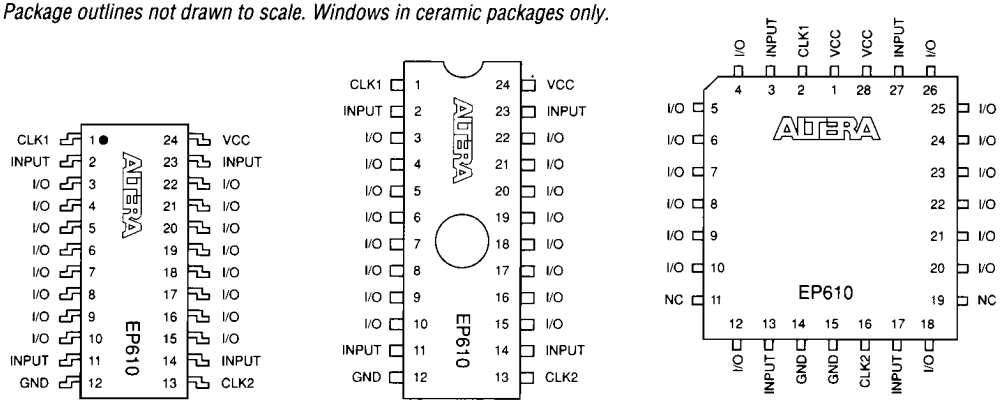
Features

- High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 83 MHz
  - Pipelined data rates up to 83 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs
- Pin-, function-, and programming file-compatible with Altera's EP610A, EP610T, and EP610 MIL-STD-883-compliant devices
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 10):
  - 24-pin small-outline integrated circuit (plastic SOIC only)
  - 24-pin dual in-line package (CerDIP and PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

Figure 10. EP610 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



General Description

The EP610 has 16 macrocells, 4 dedicated input pins, 16 I/O pins, and 2 global Clock pins (see Figure 11). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. CLOCK1 is a dedicated Clock input for the registers in macrocells 9 through 16. CLOCK2 is a dedicated Clock input for registers in macrocells 1 through 8.

Figure 11. EP610 Block Diagram

Numbers without parentheses are for DIP and SOIC packages. Numbers in parentheses are for J-lead packages.

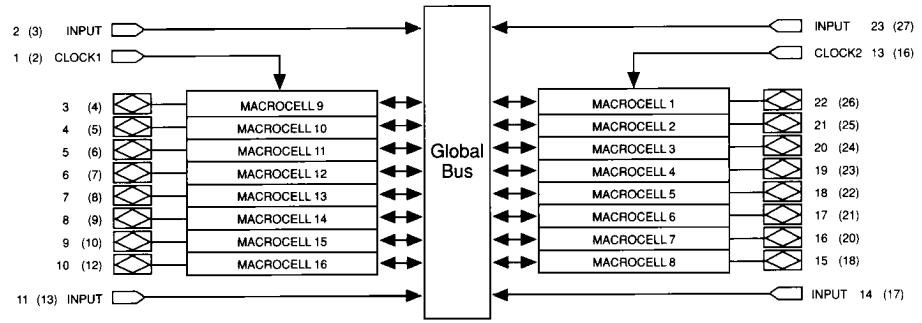
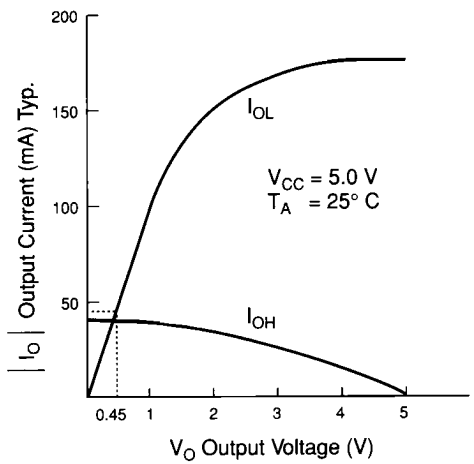


Figure 12 shows the maximum output drive characteristics of EP610 I/O pins.

Figure 12. EP610 Maximum Output Drive Characteristics

EP610-15 & EP610-20 EPLDs



EP610-25, EP610-30 & EP610-35 EPLDs

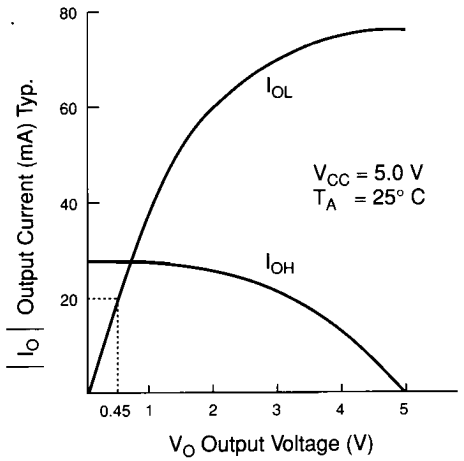
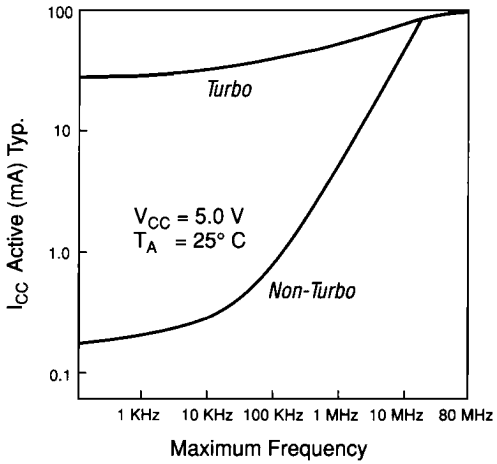


Figure 13 shows the typical supply current (I_{CC}) versus frequency of all EP610 devices.

Figure 13. EP610 I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time	*Note (3)*		100 (50)	ns
t_F	Input fall time			100 (50)	ns

DC Operating Conditions *Notes (2), (4), (5)*

Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage			–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC		2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC		3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC				0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND		–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND		–10		10	µA
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, No load, *Notes (6), (7)*			20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz			5	10 (15)	mA
I_{CC3}	V_{CC} supply current (turbo, active)	*Note (7)*	-15, -20		60	90 (115)	mA
			-25, -30, -35		45	60 (75)	mA

Capacitance *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions: EP610-15 and EP610-20 *Note (5)*

			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	20	ns
t_{PD2}	I/O input to non-registered output			17		22	20	ns
t_{PZX}	Input to output enable			15		20	20	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (10)*		15		20	20	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20	20	ns
t_{IO}	I/O input pad and buffer delay			2		2	0	ns

Global Clock Mode			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*Note (11)*	83.3		62.5		0	MHz
t_{SU}	Input setup time		9		11		20	ns
t_{H}	Input hold time		0		0		0	ns
t_{CH}	Clock high time		6		8		0	ns
t_{CL}	Clock low time		6		8		0	ns
t_{CO1}	Clock to output delay			11		13	0	ns
t_{CNT}	Minimum clock period			12		16	0	ns
f_{CNT}	Internal maximum frequency	*Note (7)*	83.3		62.5		0	MHz

Array Clock Mode			EP610-15		EP610-20		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*Note (11)*	71.4		55.6		0	MHz
t_{ASU}	Input setup time		6		8		20	ns
t_{AH}	Input hold time		6		8		0	ns
t_{ACH}	Clock high time		7		9		0	ns
t_{ACL}	Clock low time		7		9		0	ns
t_{ACO1}	Clock to output delay			15		20	20	ns
t_{ACNT}	Minimum clock period			14		18	0	ns
f_{ACNT}	Internal maximum frequency	*Note (7)*	71.4		55.6		0	MHz

AC Operating Conditions: EP610-25, EP610-30, and EP610-35 *Note (5)*

			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	30	ns
t_{PD2}	I/O input to non-registered output			27		32		37	30	ns
t_{PZX}	Input to output enable			25		30		35	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (10)*		25		30		35	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		27		32		37	30	ns
t_{IO}	I/O input pad and buffer delay			2		2		2	0	ns

Global Clock Mode			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*Note (11)*	47.6		41.7		37.0		0	MHz
t_{SU}	Input setup time		21		24		27		30	ns
t_{H}	Input hold time		0		0		0		0	ns
t_{CH}	Clock high time		10		11		12		0	ns
t_{CL}	Clock low time		10		11		12		0	ns
t_{CO1}	Clock to output delay			15		17		20	0	ns
t_{CNT}	Minimum clock period			25		30		35	0	ns
f_{CNT}	Internal maximum frequency	*Note (7)*	40.0		33.3		28.6		0	MHz

Array Clock Mode			EP610-25		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (9)*	**Unit**
f_{MAX}	Maximum frequency	*Note (11)*	47.6		41.7		37.0		0	MHz
t_{ASU}	Input setup time		8		8		8		30	ns
t_{AH}	Input hold time		12		12		12		0	ns
t_{ACH}	Clock high time		10		11		12		0	ns
t_{ACL}	Clock low time		10		11		12		0	ns
t_{ACO1}	Clock to output delay			27		32		37	30	ns
t_{ACNT}	Minimum clock period			25		30		35	0	ns
f_{ACNT}	Internal maximum frequency	*Note (7)*	40.0		33.3		28.6		0	MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP610-15 and EP610-20 EPLDs: maximum V_{PP} is 14.0 V.
(2) Numbers in parentheses are for military- and industrial-temperature-range versions.
(3) For EP610-15 and EP610-20 EPLDs: t_R and t_F = 40 ns. For EP610-15 and EP610-20 Clocks: t_R and t_F = 20 ns.
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) When the Turbo Bit is not set (non-turbo mode), an EP610 EPLD will enter standby mode if no logic transitions occur for 100 ns (after the last transition).
(7) Measured with a device programmed as a 16-bit counter. I_{CC} measured at 0° C.
(8) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. For EP610-25, EP610-30, and EP610-35 EPLDs: Pin 13 (high-voltage pin during programming) has a maximum capacitance of 50 pF; C_{IN}, C_{OUT}, and C_{CLK} = 20 pF.
(9) See "Turbo Bit" earlier in this data sheet.
(10) Sample-tested only for an output change of 500 mV.
(11) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP610-15, EP610-20, EP610-25, EP610-30, EP610-35
Industrial Temp.	(–40° C to 85° C)	EP610-20, EP610-30, EP610-35
Military Temp.	(–55° C to 125° C)	EP610-35 *Note (1)*

Note:

(1) Only military-temperature-range devices are listed. MIL-STD-883-compliant product specifications are provided in the *EP610 MIL-STD-883-Compliant EPLD Data Sheet* in this data book and in Military Product Drawings (MPDs). However, MPDs should be used to prepare Source Control Drawings (SCDs) and are available from Altera Marketing at (408) 894-7000. (For more information on MPDs and SCDs, see the *Military Products Data Sheet* in this data book.)