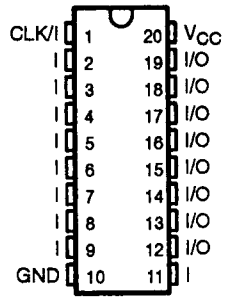
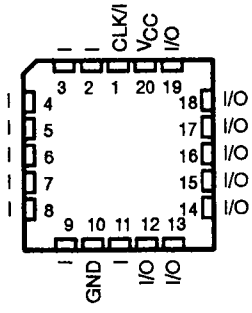
- **Programmable Replacement for Conventional TTL, 74HC, and 20-Pin PLD Family**
- **High-Voltage EPIC™ Process Allows for Higher Performance as Follows:**
  Maximum t_{pd}: -12C . . . 12 ns
  -15C . . . 15 ns
  -25I . . . 25 ns
- **User-Programmable Output Logic Macrocells Provide Flexibility in Output Types With:**
  - **Selectable for Registered or Combinational Operation**
  - **Output Polarity Control**
  - **Independently User Programmable Feedback Path**
- **Programmable Design-Security Bit Prevents Copying of Logic Stored in Device**
- **Third-Party Advanced Software Support Featuring Schematic Capture, Interactive Netlist, Boolean Equations, and State-Machine Design Entry**
- **Package Options Include:**
  - **20-pin Plastic Dual-In-Line (N)**
  - **20-pin Plastic Chip Carrier (FN)**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

general

The EP330 features advanced-CMOS speed and very low power utilizing Texas Instruments High-Voltage Enhanced-Processed Implanted CMOS (HVEPIC) process. Each output has an Output-Logic-Macrocell (OLM) configuration that allows user definition of the output type. The EP330 provides a reliable low-power substitute for numerous high-performance TTL PLDs.

The EP330 can accommodate up to 18 inputs and up to eight outputs. The 20-pin 300-mil package contains eight macrocells each using a programmable AND/fixed-OR structure. This AND-OR structure yields eight product terms for the logic function as well as an individual term for Output Enable.

AVAILABLE OPTIONS

T_A RANGE	SPEED CLASS	PACKAGE TYPE	
		PLASTIC DUAL-IN-LINE (N)	PLASTIC CHIP CARRIER (FN)
0°C to 70°C	12 ns	EP330-12CN	EP330-12CFN
	15 ns	EP330-15CN	EP330-15CFN
–40°C to 85°C	25 ns	EP330-25IN	EP330-25IFN

EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

The EP330 output-logic macrocell allows the user to configure output and feedback paths for combinational or registered operation either active high or active low. With propagation delays of 12 and15 ns, the EP330 may be configured as a low-power substitute for popular fast PLD devices such as the PAL16XXB series or the 'PAL16XX-12 and 'PAL16XX-15 series.

The CMOS EPROM technology makes it possible for the EP330 to operate at an active power-consumption level that is less than 75% of equivalent bipolar devices without sacrificing speed performance. This technology also facilitates 100% generic wafer testability using the UV-light erasable capability. As a result, designs and design modification can be quickly effected with a given EP330 without the need for post-programming testing.

Programming the EP330 is made easy by the availability of extensive third-party support for design entry, design processing, and device programming.

The EP330C is characterized for operation from 0°C to 70°C. The EP330I is characterized for operation from –40°C to 85°C.

functional description

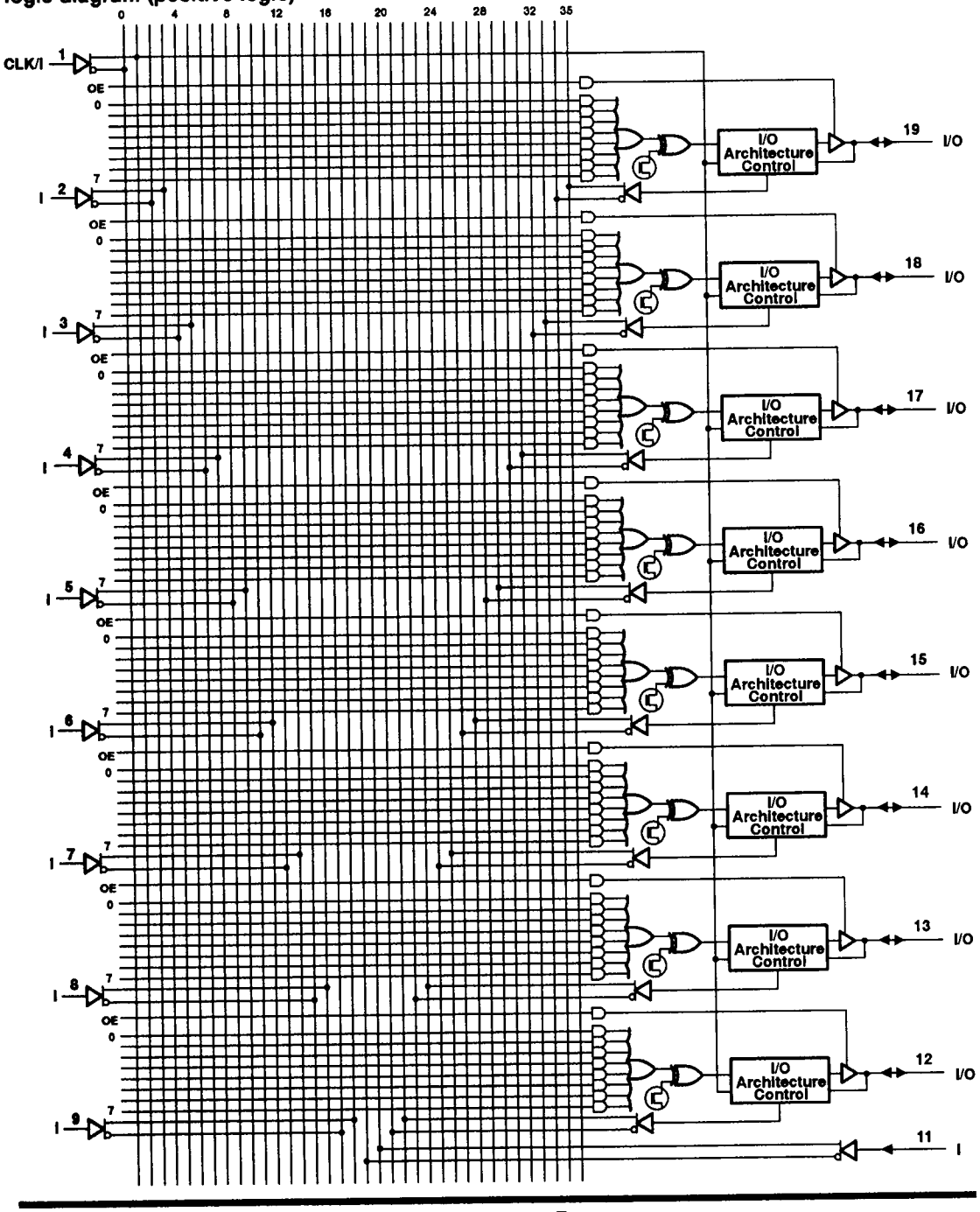
Externally, the EP330 provides ten dedicated inputs (one of which may be used as a synchronous clock input) and eight I/O pins that may be configured for input, output, or bidirectional operation.

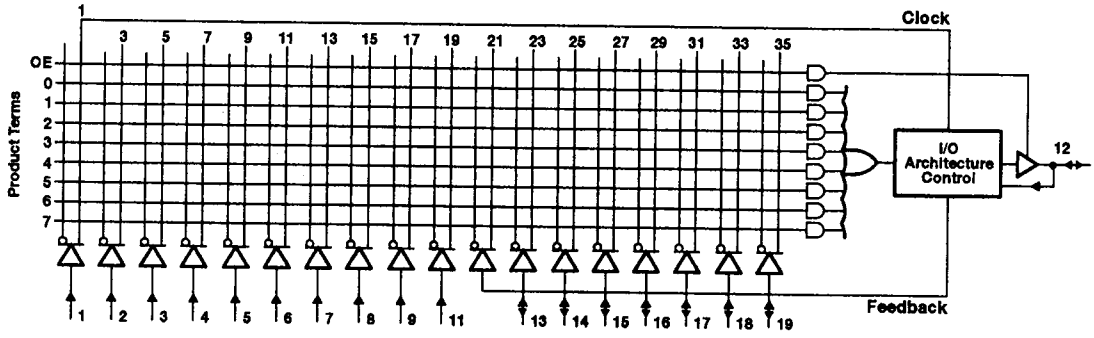
The logic diagram shows the complete EP330, while Figure 1 shows the basic EP330 macrocell. The internal architecture is organized with the familiar sum of products (AND-OR) structure. Inputs to the programmable AND array (shown running vertically in Figure 1) come from two sources: first, the true and complement of the ten dedicated input pins and second, the true and complement of the eight feedback signals, each one originating from an I/O architecture-control block. The 36-input AND array encompasses a total of 72 product terms distributed equally among the eight macrocells. Each product term (shown running horizontally in the logic diagram) represents a 36-input AND gate.

As shown in the logic diagram, the outputs of eight product terms are ORed together, then the output of the OR gate is sent as an input to an exclusive-OR gate. The purpose of this exclusive-OR gate is to allow the user to specify the polarity of the output signal by using the invert-select EPROM cell (active high if the EPROM cell is programmed and active low if it is not programmed).

The exclusive-OR output then feeds the I/O architecture control block. The control block configures the output for registered or combinational operation. In the registered configuration, the output is registered via a positive edge-triggered D-type flip-flop. In this condition, the feedback signal going to the array is also registered and comes directly from the output of the D-type flip-flop. In the combinational configuration, the output is nonregistered and the feedback signal comes directly from the I/O pin. In the erased state, the EP330 contains the same architectural characteristics as the 'PAL16L8.

logic diagram (positive logic)





NOTES: A. This diagram shows one of the eight macrocells within the EP330.
B. The double-arrow lines (⇕) show I/O feedback from a macrocell.

Figure 1. Logic Array Macrocell

output-enable product term

The output enable (OE) product term determines whether an output signal is allowed to propagate to the output pin. If the output of the OE product term is low, then the output buffer becomes a high-impedance node, thus inhibiting the output signal from reaching the output pin. For combinational configurations, this OE product term can be used to allow for true bidirectional operation.

The EP330 contains eight separate OE product terms, one per I/O pin. If it is desired that all outputs be enabled or disabled simultaneously, use an identically programmed product term at each of the outputs. If different outputs are to be enabled under different conditions, different OE product terms for each specific output may be defined.

I/O architecture

Figure 2 shows the different output configurations that can be chosen for any of the eight I/O pins on the EP330. Because of the individuality of each I/O architecture control block, both registered and combinational output can be chosen on a given EP330 device.

In the combinational configuration, either active-high or active-low output polarity can be chosen. Pin feedback or no feedback is also optional. In the registered configuration, the user has control over output polarity and may choose to use the internal feedback path or no feedback. Any I/O pin can be configured as a dedicated input by choosing no output and no feedback from the array. In the erased state, the I/O architecture is configured for a combinational active-low output with pin feedback.

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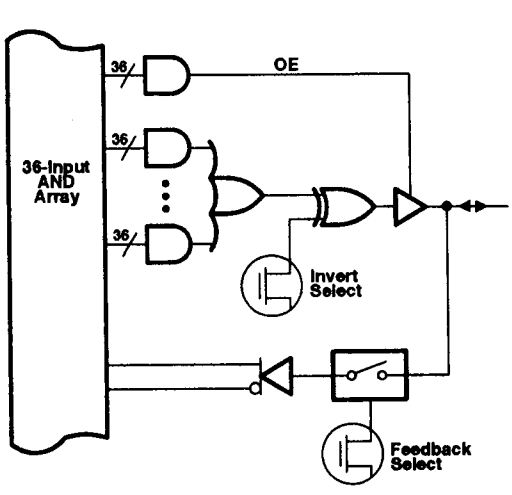
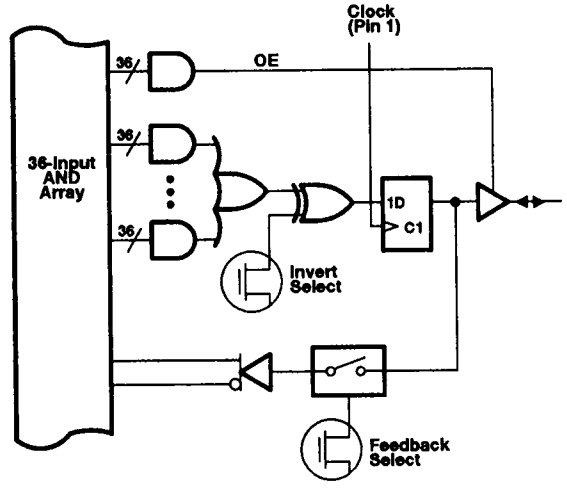


OUTPUT/POLARITY	FEEDBACK
Combinational/High	Pin, None
Combinational/Low	Pin, None
None	Pin

(a) COMBINATIONAL CONFIGURATION



OUTPUT/POLARITY	FEEDBACK
D Register/High	D Register, None
D Register/Low	D Register, None
None	D Register

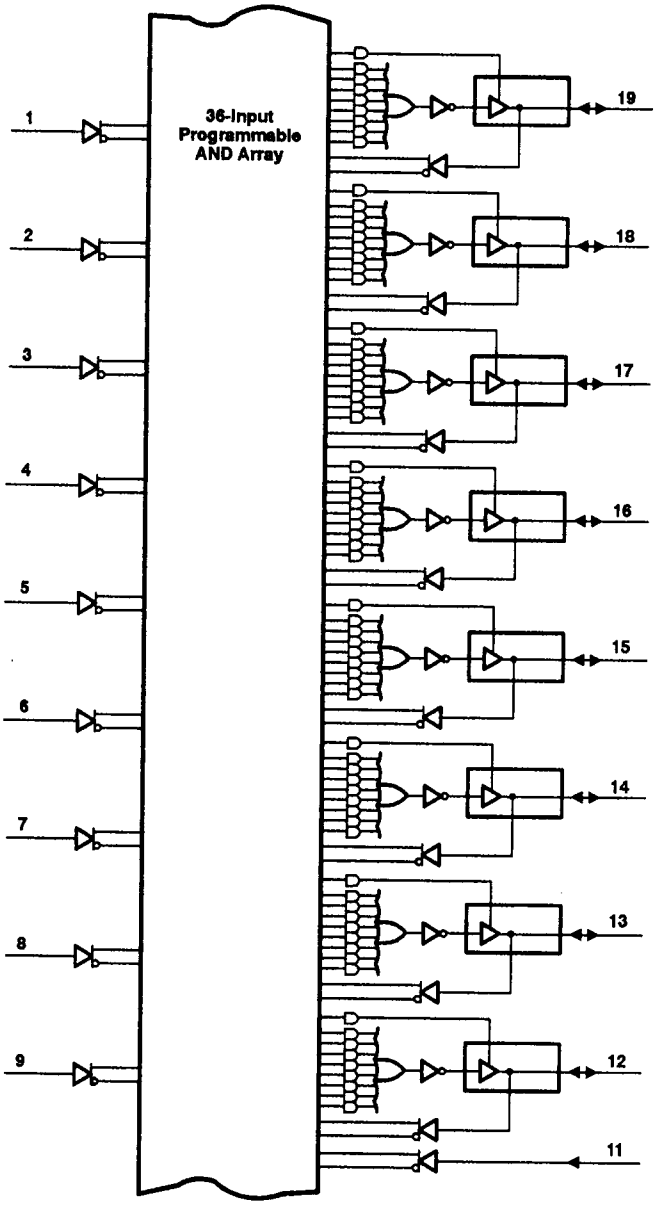
(b) REGISTERED CONFIGURATION

Figure 2. I/O Configurations

PLD compatibility

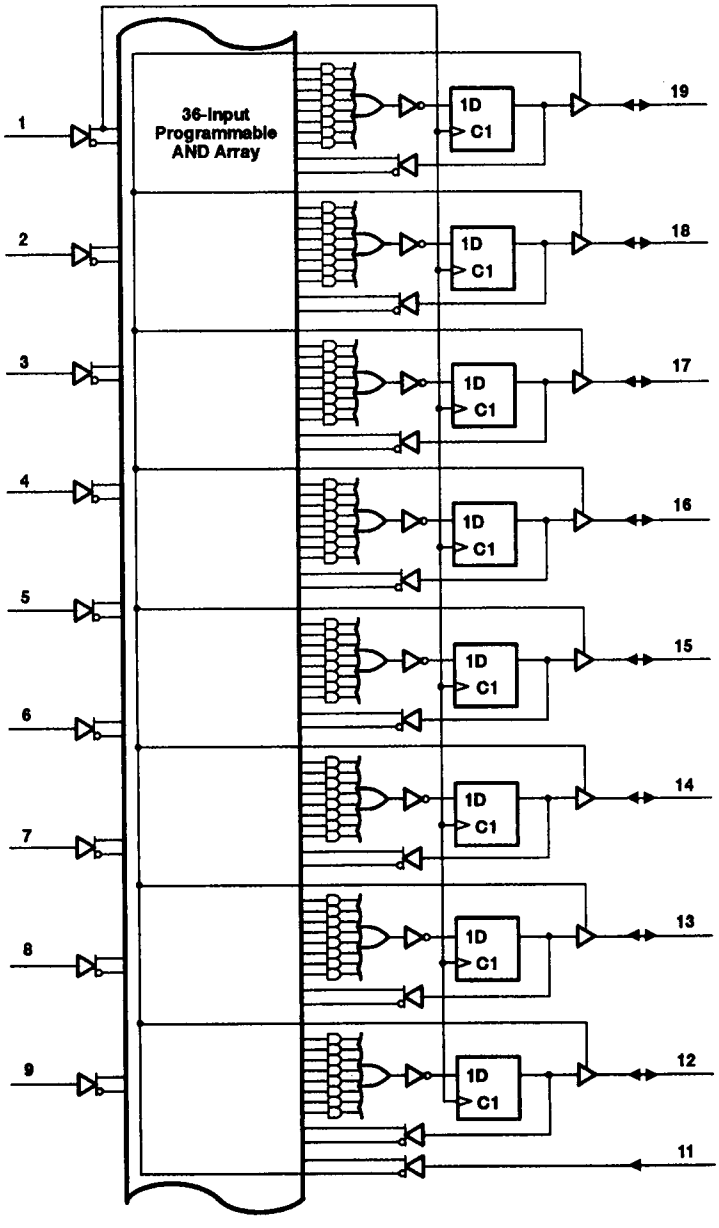
Figures 2(a) and 2(b) show how an EP330 can be configured as a drop-in replacement for two commonly used members of the 20-pin PLD family: the 'PAL16L8 and the 'PAL16R8. When configured in these manners, the EP330 is both a functional replacement, as well as a pin-to-pin replacement, for the 'PAL16L8 and 'PAL16R8.

Tables 1 and 2 provide additional information concerning the EP330 as a replacement for the 20-pin PLD family of devices.



- Invert Select EPROM cell is in the erased state providing active-low outputs.
- Combinational Mode is chosen providing Combinational Output with Input (Pin) Feedback.
- 8-product-term OR gate compared to 7-product-term OR gate on 'PAL16L8.
- Pin feedback to the array at 12 through 19 is not available in 'PAL16L8.

Figure 3. EP330 Configuration for Replacing a 'PAL16L8



- Invert Select EPROM cell is in the erased state providing active-low outputs.
- Registered Mode is chosen providing Registered Output with Registered Feedback.
- Complement of pin 11 is used as common OE term for all eight output pins.

Figure 4. EP330 Configuration for Replacing a 'PAL16R8

Table 1. Configurations for 20-Pin PLD Replacement

PLD PART NUMBER	EP330 PIN NUMBER	EP330 MACROCELL NUMBER	I/O CONFIGURATION MODE	OUTPUT/ POLARITY	FEEDBACK
10H8	12-19	1-8	Combinational	Comb/High	None
10L8	12-19	1-8	Combinational	Comb/Low	None
12H6	12	8	Combinational	None	Pin
	13-18	2-7	Combinational	Comb/High	None
	19	1	Combinational	None	Pin
12L6	12	8	Combinational	None	Pin
	13-18	2-7	Combinational	Comb/Low	None
	19	1	Combinational	None	Pin
14H4	12-13	7-8	Combinational	None	Pin
	14-17	3-6	Combinational	Comb/High	None
	18-19	1-2	Combinational	None	Pin
14L4	12-13	7-8	Combinational	None	Pin
	14-17	3-6	Combinational	Comb/Low	None
	18-19	1-2	Combinational	None	Pin
16C1	12-14	6-8	Combinational	None	Pin
	15	5	Combinational	Comb/Low	None
	16	4	Combinational	Comb/High	None
	17-19	1-3	Combinational	None	Pin
16H2	12-14	6-8	Combinational	None	Pin
	15-16	4-5	Combinational	Comb/High	None
	17-19	1-3	Combinational	None	Pin
16L2	12-14	6-8	Combinational	None	Pin
	15-16	4-5	Combinational	Comb/Low	None
	17-19	1-3	Combinational	None	Pin
16H8	12	8	Combinational	Comb/High/Z	None
&	13-18	2-7	Combinational	Comb/High/Z	Comb
16HD8	19	1	Combinational	Comb/High/Z	None
16L8	12	8	Combinational	Comb/Low/Z	None
&	13-18	2-7	Combinational	Comb/Low/Z	Comb
16LD8	19	1	Combinational	Comb/Low/Z	None
16R4	12-13	7-8	Combinational	Comb/Low/Z	Comb
	14-17	3-6	Registered	Reg/Low/Z	Reg
	18-19	1-2	Combinational	Comb/Low/Z	Comb
16R6	12	8	Combinational	Comb/Low/Z	Comb
	13-18	2-7	Registered	Reg/Low/Z	Reg
	19	1	Combinational	Comb/Low/Z	Comb
16R8	12-19	1-8	Registered	Reg/Low/Z	Reg
16P8	12	8	Combinational	Comb/Option/Z	None
	13-18	2-7	Combinational	Comb/Option/Z	Comb
	19	1	Combinational	Comb/Option/Z	None
16RP4	12-13	7-8	Combinational	Comb/Option/Z	Comb
	14-17	3-6	Registered	Reg/Option/Z	Reg
	18-19	1-2	Combinational	Comb/Option/Z	Comb
16RP6	12	8	Combinational	Comb/Option/Z	Comb
	13-18	2-7	Registered	Re/Option/Z	Reg
	19	1	Combinational	Comb/Option/Z	Comb
16RP8	12-19	1-8	Registered	Reg/Option/Z	Reg

Table 2. Device Specifications†

SYMBOL	PARAMETER	HIGH-SPEED EPLD		HIGH-SPEED PLD SERIES '16XXB/-15	
		EP330-12C	EP330-15C	'PAL16L8B/-15	'PAL16R8B/-15
I_{CC}	Supply current active	75 mA	75 mA	180 mA	180 mA
t_{pd}	Input to nonregistered output	12 ns	15 ns	15 ns	N/A
t_{CO1}	Clock to output delay	8 ns	10 ns	N/A	12 ns
t_{su}	Input setup time	6 ns	8 ns	N/A	15 ns
f_{max}	Max frequency	125 MHz	100 MHz	N/A	37 MHz

† Over commercial temperature range

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} ($t \leq 20$ ns) ..... −2 V to 7 V
Programming supply voltage range, V_{PP} ..... −0.3 V to 14 V
Instantaneous programming supply voltage range, V_{PP} ($t \leq 20$ ns) ..... −2 V to 14 V
Input voltage range, V_I ..... −0.3 V to 7 V
Instantaneous input voltage range, V_I ($t \leq 20$ ns) ..... −2 V to 7 V
V_{CC} or GND current range ..... −160 mA to 160 mA
Operating free-air temperature range, T_A ..... −65°C to 135°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: All voltage values are with respect to GND terminal.

recommended operating conditions

		EP330-12C		EP330-15C		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.75	5.25	4.75	5.25	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_{IH}	High-level input voltage	2	V_{CC}+0.3	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 2)	−0.3	0.8	−0.3	0.8	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
t_w	Pulse duration, CLK high or low	4		5		ns
t_{su}	Setup time, input	6		8		ns
t_h	Hold time, input	0		0		ns
t_r	Rise time, input		20		20	ns
t_f	Fall time, input		20		20	ns
T_A	Operating free-air temperature	0	70	0	70	°C

NOTE 2: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	EP330-12C EP330-15C			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, I_{OH} = −12 mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 24 mA			0.5	V
I_I	Input current	V_I = 5.25 V or GND			±10	µA
I_{OZ}	Off-state output current	V_{CC} = 5.25 V, V_O = V_{CC} or GND			±10	µA
I_{CC}	Supply current	f = 1 MHz, No load, Programmed as an 8-bit counter		45	75	mA
C_i‡	Input capacitance	V_{CC} = 5 V, V_I = 0, f = 1 MHz			10	pF
C_o	Output capacitance	V_{CC} = 5 V, V_O = 0, f = 1 MHz			15	pF
C_{clk}	Clock capacitance	V_{CC} = 5 V, V_{CLK} = 0, f = 1 MHz			10	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The input capacitance at pin 11 is 20 pF maximum when used as a programming pin and with V_{PP} = 14 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 5)

PARAMETER†			EP330-12C		EP330-15C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}‡	Maximum frequency	With no feedback	125		100		MHz
		With internal feedback	100		100		
		With external feedback	71.4		55.6		
t_{pd1}	Input to nonregistered output delay (see Note 3)			12		15	ns
t_{pd2}	I/O to nonregistered output delay (see Note 3)			13		16	ns
t_{io}	I/O input and buffer delay (see Note 3)			1		1	ns
t_{co}	Clock input to registered output delay (see Note 3)			8		10	ns
t_{PZX}	Output enable time (see Note 4)			12		15	ns
t_{PXZ}	Output disable time (see Note 4)			12		15	ns
t_{cnt}	Minimum clock period (internal)			10		12	ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

‡ f_{max} with no feedback $= \frac{1}{t_w \text{ high} + t_w \text{ low}}$, f_{max} with internal feedback $= \frac{1}{t_{cnt}}$,

f_{max} with external feedback $= \frac{1}{t_{su} + t_{co}}$.

f_{max} with internal feedback is programmed as an 8-bit counter.

NOTES: 3. This parameter is measured with only one output switching.
4. This is for an output voltage change of 500 mV.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 2)	−0.3	0.8	V
V_O	Output voltage	0	V_{CC}	V
t_w	Pulse duration, CLK high or low	12		ns
t_{su}	Setup time, input	15		ns
t_h	Hold time, input	0		ns
t_r	Rise time, input		20	ns
t_f	Fall time, input		20	ns
T_A	Operating free-air temperature	−40	85	°C

NOTE 2: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −12 mA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 24 mA				0.5	V
I_I	Input current	V_I = 5.5 V or GND					±10	µA
I_{OZ}	Off-state output current	V_{CC} = 5.5 V,	V_O = V_{CC} or GND				±10	µA
I_{CC}	Supply current	f = 1 MHz,	No load,	Programmed as an 8-bit counter		45	75	mA
C_i	Input capacitance	V_{CC} = 5 V,	V_I = 2 V,	f = 1 MHz			10	pF
C_o	Output capacitance	V_{CC} = 5 V,	V_O = 2 V,	f = 1 MHz			15	pF
C_{clk}	Clock capacitance	V_{CC} = 5 V,	V_{CLK} = 2 V,	f = 1 MHz			10	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 5)

PARAMETER‡			MIN	MAX	UNIT
f_{max}§	Maximum frequency	With no feedback	41.6		MHz
		With internal feedback	41.6		
		With external feedback	28.5		
t_{pd1}	Input to nonregistered output delay (see Note 3)			25	ns
t_{pd2}	I/O to nonregistered output delay (see Note 3)			26	ns
t_{io}	I/O input and buffer delay (see Note 3)			1	ns
t_{co}	Clock input to registered output delay (see Note 3)			15	ns
t_{PZX}	Output enable time (see Note 4)			25	ns
t_{PXZ}	Output disable time (see Note 4)			25	ns
t_{cnt}	Minimum clock period (internal)			24	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

§ f_{max} with no feedback = $\frac{1}{t_w \text{ high} + t_w \text{ low}}$, f_{max} with internal feedback = $\frac{1}{t_{cnt}}$,

f_{max} with external feedback = $\frac{1}{t_{su} + t_{co}}$.

f_{max} with internal feedback is programmed as an 8-bit counter.

NOTES: 3. This parameter is measured with only one output switching.

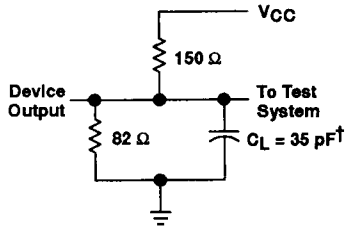
4. This is for an output voltage change of 500 mV.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

functional testing

The EP330 is functionally tested through complete testing of each programmable EPROM bit and all internal logic elements, thus ensuring 100% programming yield.



† Includes probe and circuit capacitance. Equivalent loads may be used for testing.

Figure 5. Dynamic Test Circuit

design security

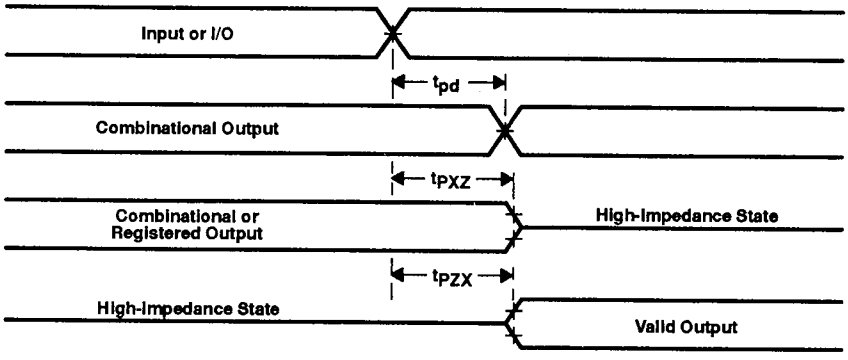
The EP330 contains a programmable design-security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. Therefore, a very high level of design control is achieved since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset by erasing the cells in the device.

latch-up

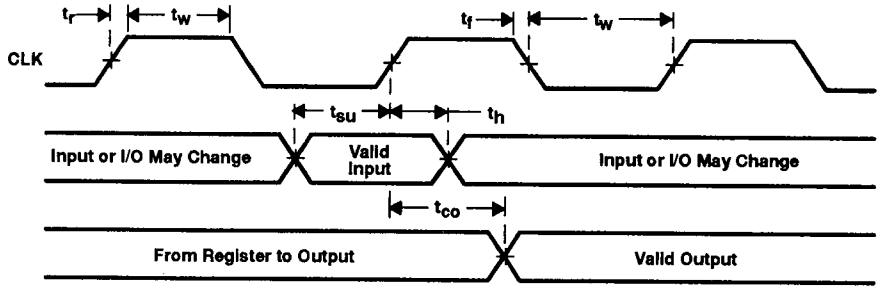
The EP330 input, I/O, and clock pins have been carefully designed to resist the latch-up that is inherent in CMOS structures. The EP330 pins will not latch up for input voltages between –1 V and V_{CC} + 1 V with currents up to 250 mA. During transitions, the inputs may undershoot to –2 V for periods of less than 20 ns.

Although the programming pin (pin 11) is designed to resist latch-up to the 13.5-V limit, during positive-current latch-up testing, the verify mode (pin 1) and program mode (pin 11) can be inadvertently entered into, causing current flow in the pins. This should not be construed as latch-up.

PARAMETER MEASUREMENT INFORMATION



(a) COMBINATIONAL MODE



(b) SYNCHRONOUS CLOCK MODE

NOTES: A. Rise time (t_r) and fall time (t_f) < 3 ns
B. t_w is measured at 0.3 V and 2.7 V. All other timing is measured at 1.5 V, except t_{PZX} and t_{PXZ} which are measured for an output voltage change of 500 mV.
C. Input voltage levels at 0 V and 3 V

Figure 6. Voltage Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREQUENCY

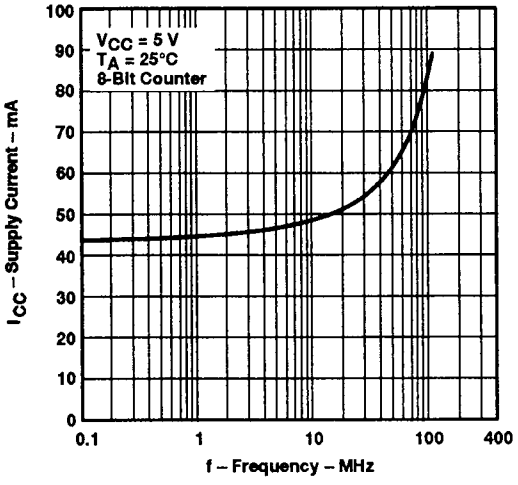


Figure 7

CHANGE IN PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

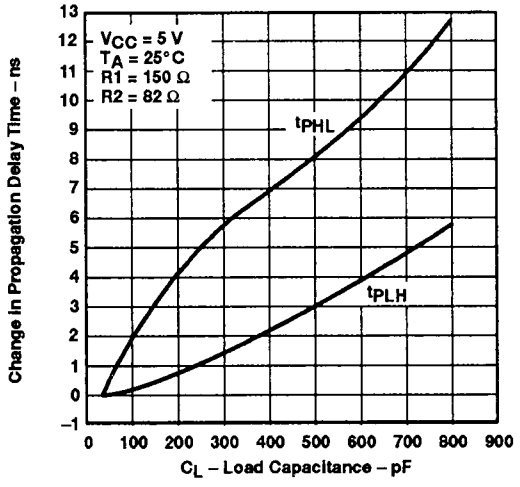


Figure 8

CHANGE IN PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

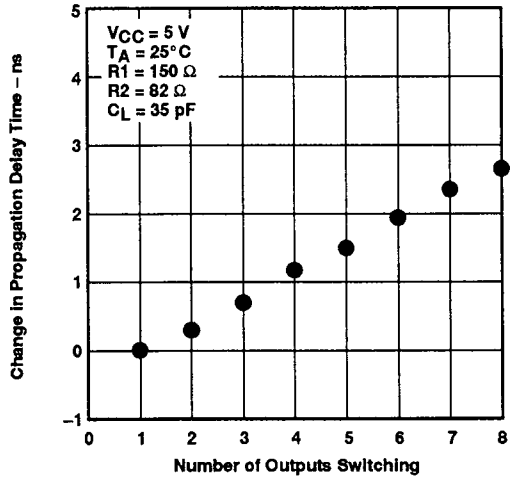


Figure 9