Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

EP330 EPLD

High-Performance 8-Macrocell Device

September 1991, ver. 2 **Data Sheet**

Features

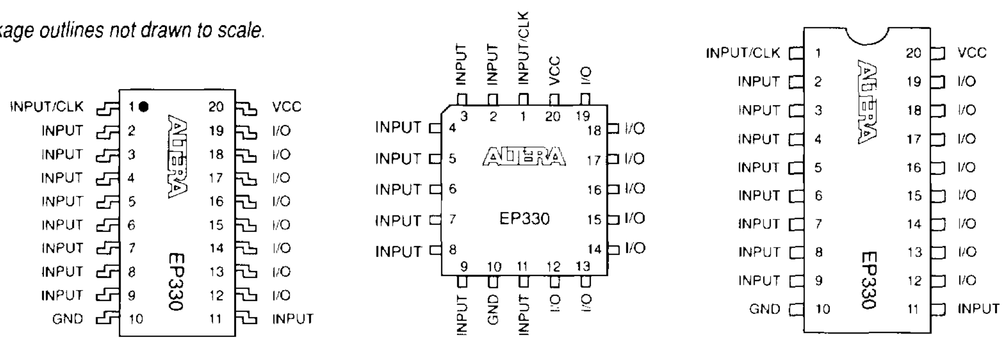
- High-performance 8-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 12 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 125 MHz
- Low power; I_{CC} = 45 mA (typical)
- Available in one-time-programmable (OTP) plastic chip carrier packages
  - 20-pin dual in-line package (PDIP)
  - 20-pin J-lead chip carrier (PLCC)
  - 20-pin, 300-mil small-outline IC (SOIC)
- Macrocell flip-flops can be individually programmed for registered or combinatorial operation
- Direct replacement for GAL 16V8 and most 20-pin PAL devices
- "Quiet" outputs minimize output switching noise found in other high-speed CMOS devices
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP330 Erasable Programmable Logic Device (EPLD) provides a high-speed, low-power, pin-compatible replacement for 20-pin programmable logic devices such as PALs and GALs. The EP330 EPLD is available in 20-pin OTP plastic DIP, J-lead, and SOIC packages. See Figure 1.

Figure 1. EP330 Package Pin-Out Diagrams

Package outlines not drawn to scale.



SOIC J-Lead DIP

The EP330 EPLD can accommodate up to 18 inputs and 8 outputs. Each of the 8 macrocells contains a programmable-AND/fixed-OR structure that implements logic with up to 8 product terms. An additional product term in each macrocell controls Output Enable.

Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in active-high and active-low modes. Thus, EP330 devices may be configured as drop-in replacements for PAL and GAL devices such as the 16R8 and 16V8. See *Application Note 2* for more information.

The EP330 CMOS EPROM technology reduces active power consumption to less than 50% of the power required by equivalent bipolar devices, without sacrificing speed. This reduced power consumption makes these EPLDs highly desirable for a wide range of applications. Additionally, EP330 EPLDs are 100% generically testable.

Logic is implemented with Altera's MAX+PLUS II or A+PLUS development systems. Both systems support schematic capture, Boolean equation, state machine, truth table, and netlist design entry methods. MAX+PLUS II also provides the Altera Hardware Description Language (AHDL), waveform design entry, and an EDIF 2 0 0 netlist interface. After the design is entered, the software automatically translates the input files into logic equations, performs Boolean minimization, and fits the design into the EPLD. MAX+PLUS II automatically partitions larger designs into multiple EPLDs. The device(s) can then be programmed in seconds at the designer's desktop to create customized working silicon. In addition, extensive third-party support exists for design entry, design processing, and device programming.

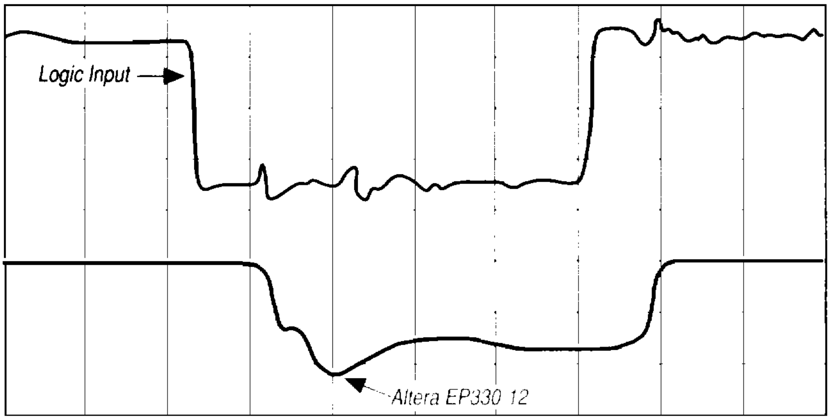
EP330 EPLD Output Characteristics

The EP330 combines high performance with low noise. For example, Figure 2 shows the switching performance of the EP330-12, Altera's 12-ns version of the EP330 EPLD. The EPLD's "quiet" outputs allow designs to run fast with high system reliability. In addition, enhanced output current capability (I_{OL} = 24 mA) allows the EP330 to directly integrate designs requiring high-current drive, such as bus interfaces. The EP330 EPLD is available with t_{PD} values of 12 ns and 15 ns.

Functional Description

The EP330 EPLD uses CMOS EPROM technology to configure connections in a programmable-AND logic array. EPROM connections are also used to control the output/feedback options, such as registered or combinatorial feedback, in active-high or active-low modes.

Figure 2. EP330-12 Output Switching Performance

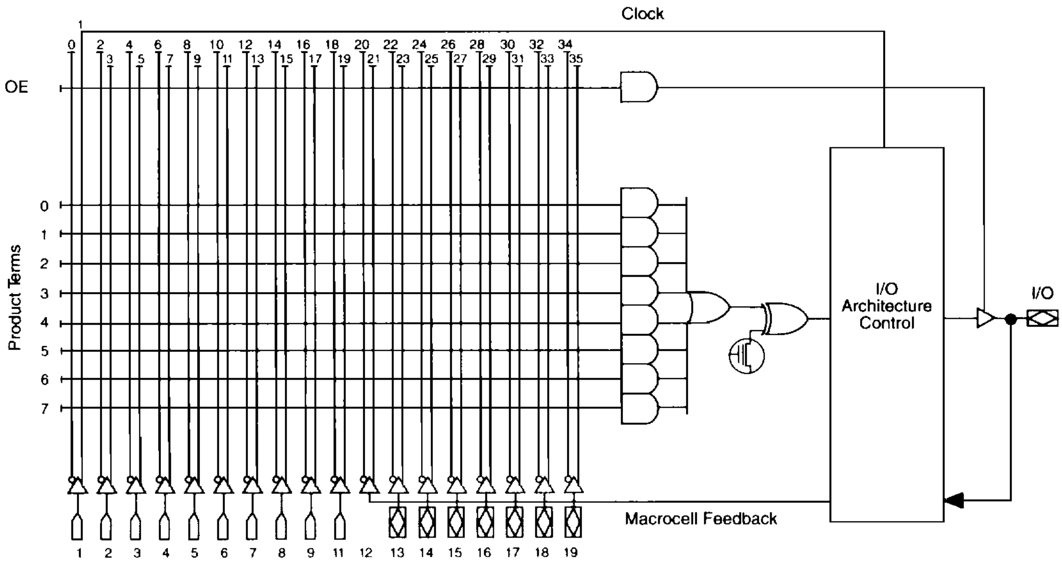


Timebase = 10.0 ns/division

Channel 1 = 1.000 V/division
Channel 2 = 2.000 V/division

An EP330 EPLD has ten dedicated data inputs and eight I/O pins that can be configured for input, output, or bidirectional operation. Figure 3 shows the EP330 macrocell.

Figure 3. EP330 Macrocell



The EP330 block diagram is shown in Figure 4. The internal architecture of this device has a sum-of-products (AND/OR) structure. Inputs to the programmable-AND array come from the true and complement signals of the 10 dedicated input pins, and the true and complement forms of the 8 feedback signals from the I/O architecture control blocks. The 36-input AND array has 72 product terms distributed equally among the 8 macrocells. Each product term represents a 36-input AND gate.

The outputs of eight product terms are ORed together; then the output of the OR gate is fed as an input to an XOR gate. The XOR function allows the designer to use the invert-select EPROM cell to specify the polarity of the output signal. If the EPROM cell is programmed, the true form of the signal (active high) is passed; if not, the complement of the signal (active low) is passed. The XOR output then feeds the I/O architecture control block, in which the output is configured for registered or combinatorial operation. In registered mode, the output is registered via a positive-edge-triggered D-type flip-flop. The feedback signal comes from the output of the flip-flop. In combinatorial mode, the output is not registered, and the feedback signal comes directly from the I/O pin.

Output Enable Product Term

The Output Enable (OE) product term determines whether an output signal will propagate to the output pin. If the output of the OE product term is high, output to the pin is enabled. If the output is low, the output buffer becomes a high-impedance node and does not allow the output signal to reach the output pin. The I/O pin can then be used as a dedicated input. This OE product term allows true bidirectional operation in combinatorial mode.

The EP330 device contains eight OE product terms, one for each I/O pin. All outputs can be enabled or disabled simultaneously by using an identically programmed product term at each of the outputs. Outputs can be enabled under other conditions by defining a different OE product term for each output.

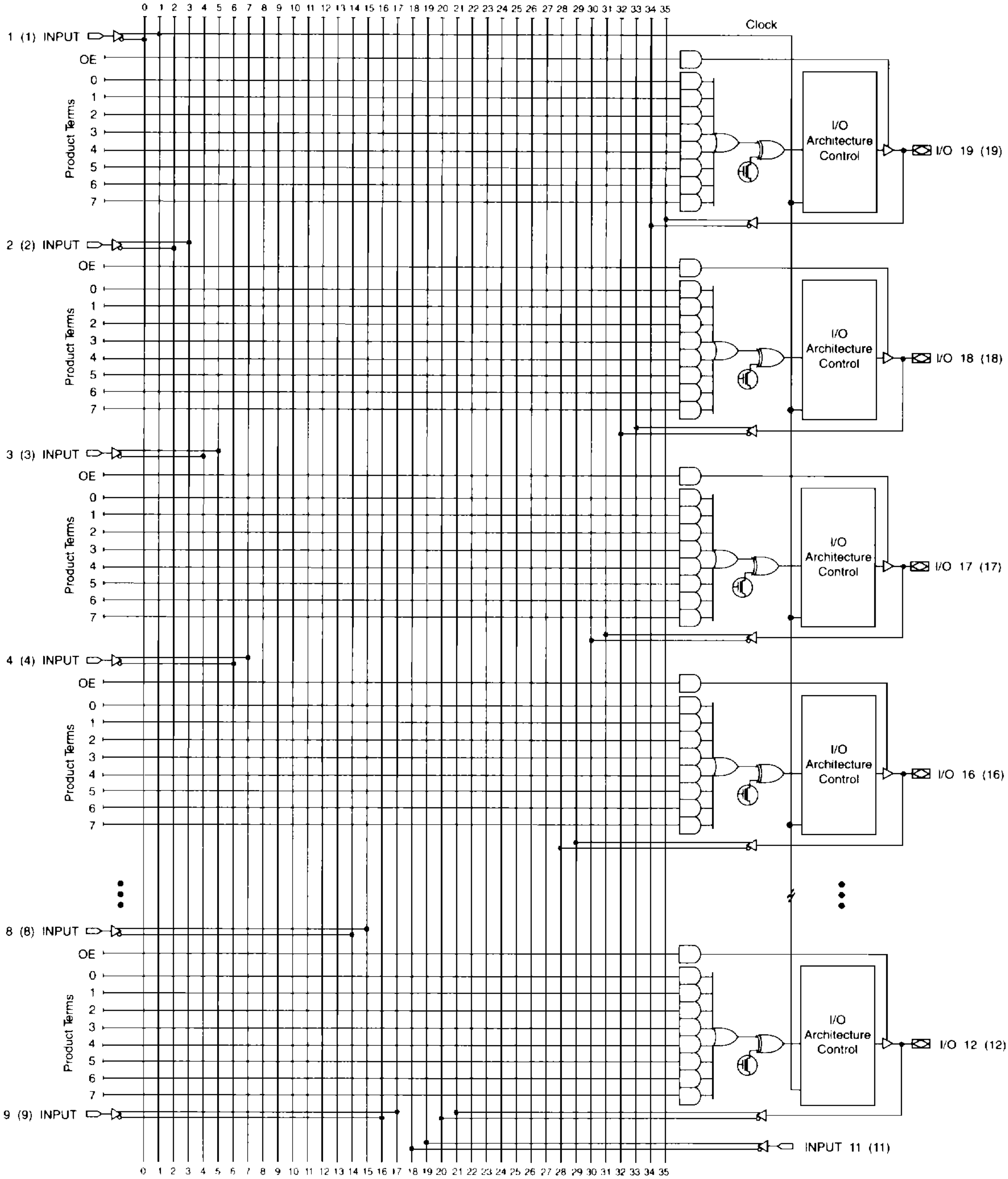
I/O Architecture

Figure 5 shows the output configurations available for the eight I/O pins. Either registered or combinatorial outputs can be individually specified for each macrocell. Any I/O pin can be configured as a dedicated input by choosing no output and pin feedback.

In combinatorial mode, active-high or active-low output polarity with pin feedback or no feedback can be chosen. In registered mode, active-high or active-low output polarity with the internal registered feedback or no feedback are available. In the erased state, the I/O architecture is configured for combinatorial active-low output with pin feedback.

Figure 4. EP330 Block Diagram

Numbers in parentheses are for J-lead packages.



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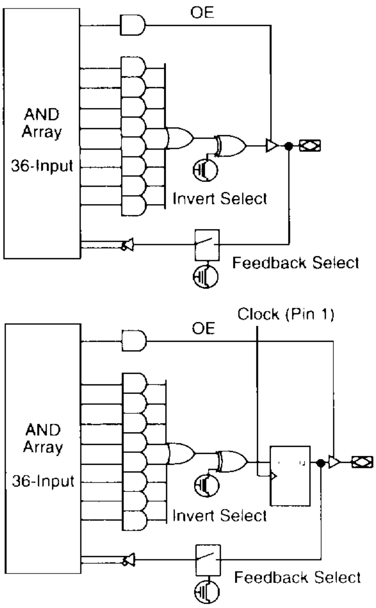
Classic EPLDs

Figure 5. EP330 I/O Configurations



Combinatorial I/O Selection

Output/Polarity	Feedback
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin

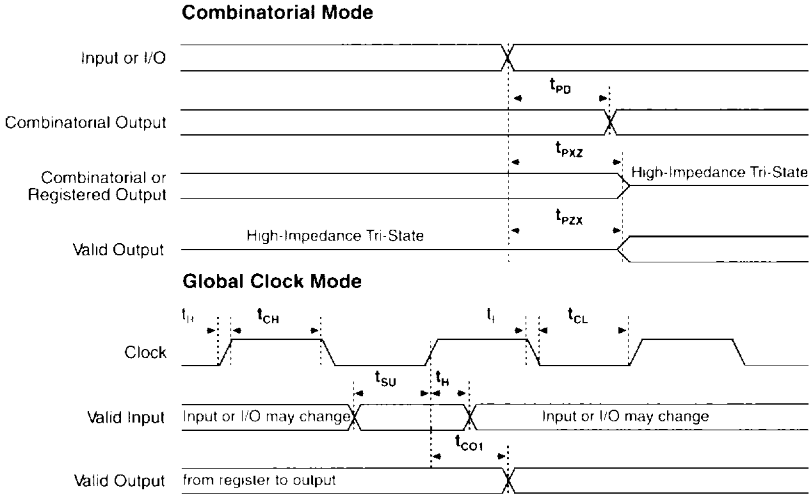
Registered I/O Selection

Output/Polarity	Feedback
D Register/High	D Register, None
D Register/Low	D Register, None
None	D Register

The switching waveforms for the EP330 EPLD are shown in Figure 6.

Figure 6. EP330 Switching Waveforms

t_R and t_F < 2 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Functional Testing

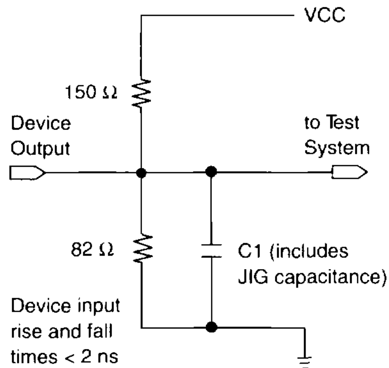
The EP330 EPLD is fully functionally tested and guaranteed through complete testing of each EPROM bit and all internal logic elements. This testing ensures a 100% programming yield.

The testing process eliminates traditional problems associated with fuse-programmed circuits. An EP330 EPLD allows test programming patterns to be used and then erased. The ability to use application-independent, general-purpose tests is called generic testing and is unique to EPLDs.

AC test measurements are performed under the conditions shown in Figure 7.

Figure 7. EP330 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.



Design Security

An EP330 EPLD contains a programmable Security Bit that controls access to the data programmed into the device. If this feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security by making programmed data within EPROM cells invisible. The Security Bit, along with all other program data, is reset by erasing the device.

Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	14.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–160	160	mA
I_{OUT}	DC output current, per pin		–50	50	mA
P_D	Power dissipation			800	mW
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	°C
T_A	Operating temperature	For industrial use	–40	85	°C
t_R	Input rise time	*See Note (2)*		20	ns
t_F	Input fall time	*See Note (2)*		20	ns

DC Operating Conditions

See Notes (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –12 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA DC			0.5	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND, No load		40	75	mA
I_{CC3}	V_{CC} supply current (active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *See Note (5)*		45	75	mA

Capacitance

See Note (6)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF

AC Operating Conditions *See Note (4)*

			EP330-12		EP330-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15	ns
t_{PD2}	I/O input to non-registered output			13		16	ns
t_{PZX}	Input to output enable			12		15	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *See Note (7)*		12		15	ns
t_{IO}	I/O input pad and buffer delay			1		1	ns

Global Clock Mode			EP330-12		EP330-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*See Note (8)*	125		100		MHz
t_{SU}	Setup time		6		8		ns
t_H	Hold time		0		0		ns
t_{CH}	Clock high time		4		5		ns
t_{CL}	Clock low time		4		5		ns
t_{CO1}	Clock to output delay			8		10	ns
t_{CNT}	Minimum clock period			10		12	ns
f_{CNT}	Internal maximum frequency	*See Note (5)*	100		83.3		MHz

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) For all clocks: t_R and t_F = 20 ns.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(5) Measured with a device programmed as an 8-bit counter.
(6) Capacitance measured at 25° C. Sample-tested only. Pin 11 (high-voltage pin during programming) has maximum capacitance of 20 pF.
(7) Sample-tested only for an output change of 500 mV.
(8) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP330-12, EP330-15
Industrial	(–40° C to 85° C)	EP330-15
Military	(–55° C to 125° C)	Consult factory

Figure 8 shows output drive characteristics for EP330 I/O pins and typical supply current versus frequency for the EP330 EPLD.

Figure 8. EP330 Output Drive Characteristics and I_{CC} vs. Frequency