Arria 10 Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® 10 devices.

Arria 10 devices are offered in extended and industrial grades. Extended devices are offered in –E1 (fastest), –E2, and –E3 speed grades. Industrial grade devices are offered in the –I1, –I2, and –I3 speed grades.

The suffix after the speed grade denotes the power options offered in Arria 10 devices.

- L—Low static power
- S—Standard power
- M—Enabled with the V_{CC} PowerManager feature (you can power V_{CC} and V_{CCP} at nominal voltage of 0.90 V or lower voltage of 0.83 V)
- V—Supported with the SmartVID feature (lowest static power)

Related Information

Arria 10 Device Overview
Provides more information about the densities and packages of devices in the Arria 10 family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria 10 devices.

Operating Conditions

Arria 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria 10 devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1: Absolute Maximum Ratings for Arria 10 Devices—Preliminary

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.50	1.21	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	–0.50	1.21	V
V_{CCERAM}	Embedded memory power supply	—	–0.50	1.36	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	—	–0.50	2.46	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	—	–0.50	2.46	V
V_{CCPGM}	Configuration pins power supply	[1]	–0.50	2.46	V
V_{CCIO}	I/O buffers power supply	3 V I/O	–0.50	4.10	V
		LVDS I/O	–0.50	2.46	V
V_{CCA_PLL}	Phase-locked loop (PLL) analog power supply	—	–0.50	2.46	V
V_{CCT_GXB}	Transmitter power	—	–0.50	1.34	V
V_{CCR_GXB}	Receiver power	—	–0.50	1.34	V
V_{CCH_GXB}	Transmitter output buffer power	—	–0.50	2.46	V
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	—	–0.50	1.27	V
V_{CCIO_HPS}	HPS I/O buffers power supply	3 V I/O	–0.50	4.10	V
		LVDS I/O	–0.50	2.46	V

(1) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Symbol	Description	Condition	Minimum	Maximum	Unit
$V_{CCIOREF\_HPS}$	HPS I/O pre-driver power supply	—	–0.50	2.46	V
V_{CCPLL_HPS}	HPS PLL power supply	—	–0.50	2.46	V
I_{OUT}	DC output current per pin	—	–25	25	mA
T_J	Operating junction temperature	—	–55	125	°C
T_{STG}	Storage temperature (no bias)	—	–65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 2.70 V for LVDS I/O can only be at 2.70 V for ~4% over the lifetime of the device.

Table 2: Maximum Allowed Overshoot During Transitions for Arria 10 Devices—Preliminary

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the `VREFP_ADC` and `VREFN_ADC` I/O pins.

Symbol	Description	Condition (V)		Overshoot Duration as % at T_J = 100°C	Unit
		LVDS I/O [2]	3 V I/O		
Vi (AC)	AC input voltage	2.50	3.80	100	%
		2.55	3.85	42	%
		2.60	3.90	18	%
		2.65	3.95	9	%
		2.70	4.00	4	%
		> 2.70	> 4.00	No overshoot allowed	%

(2) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria 10 devices.

Recommended Operating Conditions

Table 3: Recommended Operating Conditions for Arria 10 Devices—Preliminary

This table lists the steady-state voltage values expected from Arria 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum (3)	Typical	Maximum (3)	Unit
V_{CC}	Core voltage power supply	Standard and low power	0.87	0.9 (4)	0.93	V
		V_{CC} PowerManager (5)	0.8, 0.87	0.83, 0.9	0.86, 0.93	V
		SmartVID (6)	0.8	—	0.93	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	Standard and low power	0.87	0.9 (4)	0.93	V
		V_{CC} PowerManager (5)	0.8, 0.87	0.83, 0.9	0.86, 0.93	V
		SmartVID (6)	0.8	—	0.93	V
V_{CCPGM}	Configuration pins power supply	1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.2 V	1.14	1.2	1.26	V
V_{CCERAM}	Embedded memory power supply	0.9 V	0.87	0.9(4)	0.93	V

(3) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(4) You can operate –1 and –2 speed grade devices at 0.9 V or 0.95 V typical value. You can operate -3 speed grade device at only 0.9 V typical value. Core performance shown in this datasheet is applicable for the operation at 0.9 V. Operating at 0.95 V results in higher core performance and higher power consumption. For more information about the performance and power consumption of 0.95 V operation, refer to the Quartus® Prime software timing reports, PowerPlay Power Analyzer report, and Early Power Estimator (EPE).

(5) You can operate V_{CC} PowerManager devices at either 0.83 V or 0.9 V. Power V_{CC} and V_{CCP} at 0.9 V to achieve –1 speed grade performance. Power V_{CC} and V_{CCP} at 0.83 V to achieve lower performance using the lowest power.

(6) SmartVID is supported in devices with –2V and –3V speed grades only.

Symbol	Description	Condition	Minimum (3)	Typical	Maximum (3)	Unit
V_{CCBAT} (7)	Battery back-up power supply (For design security volatile key register)	1.8 V	1.71	1.8	1.89	V
		1.2 V	1.14	1.2	1.26	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	1.8 V	1.71	1.8	1.89	V
V_{CCIO}	I/O buffers power supply	3.0 V (for 3 V I/O only)	2.85	3.0	3.15	V
		2.5 V (for 3 V I/O only)	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	(8)	1.35	(8)	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	(8)	1.2	(8)	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V
V_{REFP_ADC}	Precision voltage reference for voltage sensor	—	1.2475	1.25	1.2525	V
V_I (9)	DC input voltage	3 V I/O	–0.3	—	3.3	V
		LVDS I/O	–0.3	—	2.19	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	–40	—	100	°C

(3) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(7) If you do not use the design security feature in Arria 10 devices, connect V_{CCBAT} to a 1.5-V or 1.8-V power supply. Arria 10 power-on reset (POR) circuitry monitors V_{CCBAT}. Arria 10 devices do not exit POR if V_{CCBAT} is not powered up.

(8) For minimum and maximum voltage values, refer to the I/O Standard Specifications section.

(9) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Symbol	Description	Condition	Minimum [3]	Typical	Maximum [3]	Unit
t_{RAMP} [10][11]	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Related Information

I/O Standard Specifications on page 17

Transceiver Power Supply Operating Conditions

Table 4: Transceiver Power Supply Operating Conditions for Arria 10 GX/SX Devices—Preliminary

Symbol	Description	Condition [12]	Minimum [13]	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$	Transmitter power supply	Chip-to-Chip ≤ 17.4 Gbps Or Backplane [14] ≤ 16.0 Gbps	1.0	1.03	1.06	V
		Chip-to-Chip ≤ 11.3 Gbps Or Backplane [14] ≤ 10.3125 Gbps	0.92	0.95	0.98	V

(3) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(10) This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

(11) t_{ramp} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

(12) These data rate ranges vary depending on the transceiver speed grade. Refer to Transceiver Performance for Arria 10 GX/SX Devices for exact data rate ranges.

(13) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(14) Backplane applications assume advanced equalization circuitry, such as decision feedback equalization (DFE), is enabled to compensate for signal impairments. Chip-to-chip links are assumed to be applications with short reach channels that do not require DFE.

Symbol	Description	Condition [12]	Minimum [13]	Typical	Maximum	Unit
$V_{CCR\_GXB[L,R]}$	Receiver power supply	Chip-to-Chip ≤ 17.4 Gbps Or Backplane [14] ≤ 16.0 Gbps	1.0	1.03	1.06	V
		Chip-to-Chip ≤ 11.3 Gbps Or Backplane [14] ≤ 10.3125 Gbps	0.92	0.95	0.98	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power	—	1.710	1.8	1.890	V

Note: Most VCCR_GXB and VCCT_GXB pins associated with unused transceiver channels can be grounded on a per-side basis to minimize power consumption. Refer to the *Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines* and the Quartus Prime pin report for information about pinning out the package to minimize power consumption for your specific design.

(12) These data rate ranges vary depending on the transceiver speed grade. Refer to Transceiver Performance for Arria 10 GX/SX Devices for exact data rate ranges.

(13) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 5: Transceiver Power Supply Operating Conditions for Arria 10 GT Devices—Preliminary

Symbol	Description	Condition [15]	Minimum [13]	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$	Transmitter power supply	Chip-to-Chip < 28.3 Gbps [16] Or Backplane [14] < 17.4 Gbps	1.10	1.12	1.14	V
		Chip-to-Chip < 15 Gbps Or Backplane [14] < 14.2 Gbps	1.0	1.03	1.06	V
		Chip-to-Chip < 11.3 Gbps Or Backplane [14] < 10.3125 Gbps	0.92	0.95	0.98	V
$V_{CCR\_GXB[L,R]}$	Receiver power supply	Chip-to-Chip < 28.3 Gbps Or Backplane [14] < 17.4 Gbps	1.10	1.12	1.14	V
		Chip-to-Chip < 15 Gbps Or Backplane [14] < 14.2 Gbps	1.0	1.03	1.06	V
		Chip-to-Chip < 11.3 Gbps Or Backplane [14] < 10.3125 Gbps	0.92	0.95	0.98	V

[15] These data rate ranges vary depending on the transceiver speed grade. Refer to Transceiver Performance for Arria 10 GT Devices table for exact data rate ranges.

Symbol	Description	Condition [15]	Minimum [13]	Typical	Maximum	Unit
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power supply	—	1.710	1.8	1.890	V

Related Information

- **Transceiver Performance for Arria 10 GT Devices** on page 26
  Provides the data rate ranges for different transceiver speed grades.
- **Transceiver Performance for Arria 10 GX/SX Devices** on page 23
  Provides the data rate ranges for different transceiver speed grades.
- **Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines**

HPS Power Supply Operating Conditions

Table 6: HPS Power Supply Operating Conditions for Arria 10 SX Devices—Preliminary

This table lists the steady-state voltage and current values expected from Arria 10 system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Arria 10 Devices table for the steady-state voltage values expected from the FPGA portion of the Arria 10 SoC devices.

Symbol	Description	Condition	Minimum [17]	Typical	Maximum [17]	Unit
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	HPS processor speed = 1.2 GHz	0.87	0.9	0.93	V
		HPS processor speed = 1.5 GHz, –1 speed grade	0.92	0.95	0.98	V
V_{CCIO_HPS}	HPS I/O buffers power supply	3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V

(15) These data rate ranges vary depending on the transceiver speed grade. Refer to Transceiver Performance for Arria 10 GT Devices table for exact data rate ranges.
(16) 28.3 Gbps is the maximum data rate for GT channels. 17.4 Gbps is the maximum data rate for GX channels.
(17) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol	Description	Condition	Minimum (17)	Typical	Maximum (17)	Unit
$V_{CCIOREF\_HPS}$	HPS I/O pre-driver power supply	—	1.71	1.8	1.89	V
V_{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V

Related Information

Recommended Operating Conditions on page 4
Provides the steady-state voltage values for the FPGA portion of the device.

DC Characteristics

The OCT variation after power-up calibration specifications will be available in a future release of the *Arria 10 Device Datasheet*.

Supply Current and Power Consumption

Altera offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Quartus Prime PowerPlay Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Quartus Prime PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

Related Information

- **PowerPlay Early Power Estimator User Guide**
  Provides more information about power estimation tools.
- **PowerPlay Power Analysis chapter, Quartus Prime Handbook**
  Provides more information about power estimation tools.

(17) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

I/O Pin Leakage Current

Table 7: I/O Pin Leakage Current for Arria 10 Devices—Preliminary

If $V_O = V_{CCIO}$ to $V_{CCIOMAX}$, 300 µA of leakage current per I/O is expected.

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–80	80	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–80	80	µA

Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 8: Bus Hold Parameters for Arria 10 Devices—Preliminary

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8 (18), 26 (19)	—	12 (18), 32 (19)	—	30 (18), 55 (19)	—	60	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8 (18), –26 (19)	—	–12 (18), –32 (19)	—	–30 (18), –55 (19)	—	–60	—	–70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	µA

(18) This value is only applicable for LVDS I/O bank.
(19) This value is only applicable for 3 V I/O bank.

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.38	1.13	0.68	1.07	0.70	1.7	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 9: OCT Calibration Accuracy Specifications for Arria 10 Devices—Preliminary

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
48-Ω, 60-Ω, 80-Ω, and 240-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
25-Ω R_S	Internal series termination with calibration	V_{CCIO} = 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R_S	Internal series termination with calibration	V_{CCIO} = 1.8, 1.5, 1.2	±15	±15	±15	%

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
34-Ω, 40-Ω, 48-Ω, and 60-Ω R_S	Internal series termination with calibration (34-Ω, 40-Ω, 48-Ω, and 60-Ωsetting)	POD12 I/O standard, V_{CCIO} = 1.2	±15	±15	±15	%
34-Ω, 40-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 40-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω setting)	POD12 I/O standard, V_{CCIO} = 1.2	±15	±15	±15	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	–10 to +40	–10 to +40	–10 to +40	%
30-Ω and 40-Ω R_T	Internal parallel termination with calibration (30-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	–10 to +40	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8, 1.5, 1.2	–10 to +40	–10 to +40	–10 to +40	%

OCT Without Calibration Resistance Tolerance Specifications

Table 10: OCT Without Calibration Resistance Tolerance Specifications for Arria 10 Devices—Preliminary

This table lists the Arria 10 OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	Resistance Tolerance			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 2.5, 3.0	–40 to +30	± 40	± 40	%
		V_{CCIO} = 1.8, 1.5	–50 to +30	± 50	± 50	%
		V_{CCIO} = 1.2	–50 to +30	± 50	± 50	%
34-Ω R_S	Internal series termination without calibration (34-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–50 to +30	± 50	± 50	%
		V_{CCIO} = 1.2	–50 to +30	± 50	± 50	%
		POD12 I/O standard	–50 to +30	± 50	± 50	%

Symbol	Description	Condition (V)	Resistance Tolerance			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
40-Ω R_S	Internal series termination without calibration (40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–50 to +30	± 50	± 50	%
		V_{CCIO} = 1.2	–50 to +30	± 50	± 50	%
		POD12 I/O standard	–50 to +30	± 50	± 50	%
48-Ω R_S	Internal series termination without calibration(48-Ω setting)	V_{CCIO} = 1.2	–50 to +30	± 50	± 50	%
		POD12 I/O standard	–50 to +30	± 50	± 50	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	VCCIO = 2.5, 3.0	–40 to +30	± 40	± 40	%
		V_{CCIO} = 1.8, 1.5	–50 to +30	± 50	± 50	%
		V_{CCIO} = 1.2	–50 to +30	± 50	± 50	%
60-Ω R_S	Internal series termination without calibration (60-Ω setting)	V_{CCIO} = 1.2	–50 to +30	± 50	± 50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 1.8, 1.5	± 25	± 35	± 40	%
120-Ω R_S	Internal series termination without calibration (120-Ω setting)	V_{CCIO} = 1.2	–50 to +30	± 50	± 50	%

Figure 1: Equation for OCT Variation Without Recalibration—Preliminary

$$R_{OCT} = R_{SCAL}\left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle\right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

Pin Capacitance

Table 11: Pin Capacitance for Arria 10 Devices—Preliminary

Symbol	Description	Value	Unit
C_{IO_COLUMN}	Input capacitance on column I/O pins	2.5	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	2.5	pF

Internal Weak Pull-Up and Weak Pull-Down Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up. The weak pull-down feature is only available for the pins as described in the Internal Weak Pull-Down Resistor Values for Arria 10 Devices table.

Table 12: Internal Weak Pull-Up Resistor Values for Arria 10 Devices—Preliminary

Symbol	Description	Condition (V) [20]	Value [21]	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 2.5 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

Table 13: Internal Weak Pull-Down Resistor Values for Arria 10 Devices—Preliminary

Pin Name	Description	Condition (V)	Value [21]	Unit
`nIO_PULLUP`	Dedicated input pin that determines the internal pull-ups on user I/O pins and dual-purpose I/O pins.	V_{CC} = 0.9 ±3.33%	25	kΩ
`TCK`	Dedicated JTAG test clock input pin.	V_{CCPGM} = 1.8 ±5 %	25	kΩ
		V_{CCPGM} = 1.5 ±5%	25	kΩ
		V_{CCPGM} = 1.2 ±5%	25	kΩ
`MSEL[0:2]`	Configuration input pins that set the configuration scheme for the FPGA device.	V_{CCPGM} = 1.8 ±5%	25	kΩ
		V_{CCPGM} = 1.5 ±5%	25	kΩ
		V_{CCPGM} = 1.2 ±5%	25	kΩ

Related Information

Arria 10 Device Family Pin Connection Guidelines

Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

(20) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(21) Valid with ±25% tolerances to cover changes over PVT.

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Arria 10 devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Related Information

Recommended Operating Conditions on page 4

Single-Ended I/O Standards Specifications

Table 14: Single-Ended I/O Standards Specifications for Arria 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} [22] (mA)	I_{OH} [22] (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.3	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.3	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

(22) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.0-V LVTTL specification (2 mA), you should set the current strength settings to 2 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 15: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135	1.283	1.35	1.418	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125	1.19	1.25	1.31	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-12	1.14	1.2	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—
POD12	1.16	1.2	1.24	0.69 × V_{CCIO}	0.7 × V_{CCIO}	0.71 × V_{CCIO}	—	V_{CCIO}	—

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 16: Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria 10 Devices—Preliminary

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} [23] (mA)	I_{OH} [23] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-12	—	V_{REF} – 0.10	V_{REF} + 0.10	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8

[23] To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} [23] (mA)	I_{OH} [23] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—
POD12	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	(0.7 – 0.15) × V_{CCIO}	(0.7 + 0.15) × V_{CCIO}	—	—

Differential SSTL I/O Standards Specifications

Table 17: Differential SSTL I/O Standards Specifications for Arria 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	0.5	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.175	—	V_{CCIO}/2 + 0.175
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	[24]	2($V_{IH(AC)}$ – V_{REF})	2(V_{REF} – $V_{IL(AC)}$)	V_{CCIO}/2 – 0.15	—	V_{CCIO}/2 + 0.15
SSTL-135	1.283	1.35	1.45	0.18	[24]	2($V_{IH(AC)}$ – V_{REF})	2($V_{IL(AC)}$ – V_{REF})	V_{CCIO}/2 – 0.15	V_{CCIO}/2	V_{CCIO}/2 + 0.15
SSTL-125	1.19	1.25	1.31	0.18	[24]	2($V_{IH(AC)}$ – V_{REF})	2($V_{IL(AC)}$ – V_{REF})	V_{CCIO}/2 – 0.15	V_{CCIO}/2	V_{CCIO}/2 + 0.15
SSTL-12	1.14	1.2	1.26	0.16	[24]	2($V_{IH(AC)}$ – V_{REF})	2($V_{IL(AC)}$ – V_{REF})	V_{REF} – 0.15	V_{CCIO}/2	V_{REF} + 0.15
POD12	1.16	1.2	1.24	0.16	—	0.3	—	V_{REF} – 0.08	—	V_{REF} + 0.08

(23) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

(24) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Differential HSTL and HSUL I/O Standards Specifications

Table 18: Differential HSTL and HSUL I/O Standards Specifications for Arria 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{DIF(AC)}$ (V)		$V_{IX(AC)}$ (V)			$V_{CM(DC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.4	—	0.78	—	1.12	0.78	—	1.12
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.68	—	0.9	0.68	—	0.9
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	0.3	V_{CCIO} + 0.48	—	0.5 × V_{CCIO}	—	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}
HSUL-12	1.14	1.2	1.3	2($V_{IH(DC)}$ – V_{REF})	2(V_{REF} – $V_{IH(DC)}$)	2($V_{IH(AC)}$ – V_{REF})	2(V_{REF} – $V_{IH(AC)}$)	0.5 × V_{CCIO} – 0.12	0.5 × V_{CCIO}	0.5 × V_{CCIO} +0.12	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}

Differential I/O Standards Specifications

Table 19: Differential I/O Standards Specifications for Arria 10 Devices—Preliminary

Differential inputs are powered by V_{CCPT} which requires 1.8 V.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) [25]			$V_{ICM(DC)}$ (V)			V_{OD} (V) [26]			V_{OCM} (V) [26]		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the CML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Transceiver Specifications for Arria 10 GX, SX, and GT Devices table.														

(25) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.
(26) R_L range: $90 \leq R_L \leq 110\ \Omega$.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) (25)			$V_{ICM(DC)}$ (V)			V_{OD} (V) (26)			V_{OCM} (V) (26)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (27)	1.71	1.8	1.89	100	V_{CM} = 1.25 V	—	0	D_{MAX} ≤700 Mbps	1.85	0.247	—	0.6	1.125	1.25	1.375
							1	D_{MAX} > 700 Mbps	1.6						
RSDS (HIO) (28)	1.71	1.8	1.89	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) (29)	1.71	1.8	1.89	200	—	600	0.4	—	1.325	0.25	—	600	1	1.2	1.4
LVPECL (30)	1.71	1.8	1.89	300	—	—	0.6	D_{MAX} ≤700 Mbps	1.7	—	—	—	—	—	—
							1	D_{MAX} > 700 Mbps	1.6						

Related Information

Transceiver Specifications for Arria 10 GX, SX, and GT Devices on page 29
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides the performance characteristics of Arria 10 core and periphery blocks for extended grade devices.

(25) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.
(26) R_L range: 90 ≤ R_L ≤ 110 Ω.
(27) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 700 Mbps and 0 V to 1.85 V for data rates below 700 Mbps.
(28) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.4 V.
(29) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.4 V to 1.325 V.
(30) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

Transceiver Performance Specifications

Transceiver Performance for Arria 10 GX/SX Devices

Table 20: Transmitter and Receiver Data Rate Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 1	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Transceiver Speed Grade 4	Transceiver Speed Grade 5 (31)	Unit
Chip-to-Chip (32)	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB}$ = 1.03 V	17.4	15	14.2	12.5	8	Gbps
	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB}$ = 0.95 V	11.3	11.3	11.3	11.3	8	Gbps
	Minimum Data Rate	1.0 (33)					Gbps
Backplane (32)	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB}$ = 1.03 V	16	14.2	12.5	10.3125	6.5536	Gbps
	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB}$ = 0.95 V	10.3125	10.3125	10.3125	10.3125	6.5536	Gbps
	Minimum Data Rate	1.0 (33)					Gbps

(31) Transceiver speed grade 5 supports PCI Express® (PCIe®) Gen3.
(32) Backplane applications assume advanced equalization circuitry, such as decision feedback equalization (DFE), is enabled to compensate for signal impairments. Chip-to-chip links are assumed to be applications with short reach channels that do not require DFE.
(33) Arria 10 transceivers can support data rates down to 125 Mbps with over sampling.

Table 21: ATX PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 1	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Transceiver Speed Grade 4	Transceiver Speed Grade 5	Unit
Supported Output Frequency	Maximum Frequency	8.7	7.5	7.1	6.25	4	GHz
	Minimum Frequency	500					MHz

Table 22: Fractional PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 1	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Transceiver Speed Grade 4	Transceiver Speed Grade 5	Unit
Supported Output Frequency	Maximum Frequency	6.25	6.25	6.25	6.25	4	GHz
	Minimum Frequency	500					MHz

Table 23: CMU PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 1	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Transceiver Speed Grade 4	Transceiver Speed Grade 5	Unit
Supported Output Frequency	Maximum Frequency	5.15625	5.15625	5.15625	5.15625	4	GHz
	Minimum Frequency	500					MHz

Related Information

Transceiver Power Supply Operating Conditions on page 6

High-Speed Serial Transceiver-Fabric Interface Performance for Arria 10 GX/SX Devices

Table 24: High-Speed Serial Transceiver-Fabric Interface Performance for Arria 10 GX/SX Devices—Preliminary

Symbol/Description	Condition (V)	Core Speed Grade with Power Options				Unit
		-E1M / -I1M	-E1L / -E1S / -I1L	-E2L / -I2L	-E3S / -I3S / M3	
20-bit interface - FIFO	V_{CC} = 0.9	516	516	400	400	MHz
20-bit interface - Registered	V_{CC} = 0.9	491	491	400	400	MHz
32-bit interface - FIFO	V_{CC} = 0.9	441	441	404	335	MHz
32-bit interface - Registered	V_{CC} = 0.9	441	441	404	335	MHz
64-bit interface - FIFO	V_{CC} = 0.9	272	272	234	222	MHz
64-bit interface - Registered	V_{CC} = 0.9	272	272	234	222	MHz
PCIe Gen3 HIP-Fabric interface	V_{CC} = 0.9	300	300	250	250	MHz
20-bit interface - FIFO	V_{CC} = 0.83	400	—	—	—	MHz
20-bit interface - Registered	V_{CC} = 0.83	400	—	—	—	MHz
32-bit interface - FIFO	V_{CC} = 0.83	335	—	—	—	MHz
32-bit interface - Registered	V_{CC} = 0.83	335	—	—	—	MHz
64-bit interface - FIFO	V_{CC} = 0.83	222	—	—	—	MHz
64-bit interface - Registered	V_{CC} = 0.83	222	—	—	—	MHz
PCIe Gen3 HIP-Fabric interface	V_{CC} = 0.83	250	—	—	—	MHz

Transceiver Performance for Arria 10 GT Devices

Table 25: Transmitter and Receiver Data Rate Performance—Preliminary

Symbol/Description	Condition		Transceiver Speed Grade 2	Transceiver Speed Grade 3	Transceiver Speed Grade 4	Unit
Chip-to-chip [34]	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB}$ = 1.12 V	GT Channel [35]	28.3/28.1 [36]	26	20	Gbps
		GX Channel	17.4	15	15	Gbps
	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB}$ = 1.03 V	GX Channel	15	14.2	12.5	Gbps
	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB}$ = 0.95 V	GX Channel	11.3	11.3	11.3	Gbps
	Minimum data rate	GT Channel GX Channel	1.0 [37]			Gbps

(34) Backplane applications assume advanced equalization circuitry, such as decision feedback equalization (DFE), is enabled to compensate for signal impairments. Chip-to-chip links are assumed to be applications with short reach channels that do not require DFE.

(35) GT channels are only available when V_{CCT_GXB} = 1.12 V and V_{CCR_GXB} = 1.12 V.

(36) To achieve 28.3 Gbps, you must use a -1 core speed grade and a -2 transceiver speed grade device configuration. To achieve 28.1 Gbps, you must use a -2 core speed grade and a -2 transceiver speed grade device configuration.

(37) Arria 10 transceivers can support data rates down to 125 Mbps with over sampling.

Symbol/Description	Condition		Transceiver Speed Grade 2	Transceiver Speed Grade 3	Transceiver Speed Grade 4	Unit
Backplane [34]	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB} = 1.12$ V	GX Channel	17.4	14.2	14.2	Gbps
	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB} = 1.03$ V	GX Channel	14.2	12.5	10.3125	Gbps
	Maximum data rate $V_{CCR\_GXB} = V_{CCT\_GXB} = 0.95$ V	GX Channel	10.3125	10.3125	10.3125	Gbps
	Minimum data rate	GX Channel	1.0 [37]			Gbps

Table 26: ATX PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Transceiver Speed Grade 4	Unit
Supported Output Frequency	Maximum frequency	14.15	13	10	GHz
	Minimum frequency	500			MHz

Table 27: Fractional PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Transceiver Speed Grade 4	Unit
Supported Output Frequency	Maximum frequency	6.25			GHz
	Minimum frequency	500			MHz

Table 28: CMU PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Transceiver Speed Grade 4	Unit
Supported Output Frequency	Maximum frequency	5.15625	5.15625	5.15625	GHz
	Minimum frequency	500			MHz

Related Information

Transceiver Power Supply Operating Conditions on page 6

High-Speed Serial Transceiver-Fabric Interface Performance for Arria 10 GT Devices

Table 29: High-Speed Serial Transceiver-Fabric Interface Performance for Arria 10 GT Devices—Preliminary

Symbol/Description	Condition (V)	Core Speed Grade with Power Options			Unit
		-1	-2	-3	
20-bit interface - FIFO	$V_{CC} = 0.9$	516	400	400	MHz
20-bit interface - Registered	$V_{CC} = 0.9$	491	400	400	MHz
32-bit interface - FIFO	$V_{CC} = 0.9$	441	404	335	MHz
32-bit interface - Registered	$V_{CC} = 0.9$	441	404	335	MHz
64-bit interface - FIFO	$V_{CC} = 0.9$	439	407	313	MHz
64-bit interface - Registered	$V_{CC} = 0.9$	439	407	313	MHz
PCIe Gen3 HIP-Fabric interface	$V_{CC} = 0.9$	300	250	250	MHz

Transceiver Specifications for Arria 10 GX, SX, and GT Devices

Table 30: Reference Clock Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grades 1, 2, 3, 4, and 5			Unit
		Min	Typ	Max	
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL			
	RX reference clock pin	CML, Differential LVPECL, and LVDS			
Input Reference Clock Frequency (CMU PLL)		61	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL PLL)		20	—	800	MHz
Rise time	20% to 80%	—	—	400	ps
Fall time	80% to 20%	—	—	400	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX reference clock pin	—	—	1.2	V
Absolute V_{MIN}	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV

Symbol/Description	Condition	Transceiver Speed Grades 1, 2, 3, 4, and 5			Unit
		Min	Typ	Max	
V_{ICM} (AC coupled)	V_{CCR_GXB} = 0.95 V	—	0.95	—	V
	V_{CCR_GXB} = 1.03 V	—	1.03	—	V
	V_{CCR_GXB} = 1.12 V	—	1.12	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) (38)	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz
	10 kHz	—	—	–100	dBc/Hz
	100 kHz	—	—	–110	dBc/Hz
	≥ 1 MHz	—	—	–120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz)	1.5 to 100 MHz (PCIe)	—	—	4.2	ps (rms)
R_{REF}	—	—	2.0 k ±1%	—	Ω
$T_{SSC\text{-}MAX\text{-}PERIOD\text{-}SLEW}$	Max SSC df/dt			0.75	

Table 31: Transceiver Clocks Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grades 1, 2, 3, 4, and 5			Unit
		Min	Typ	Max	
CLKUSR pin for transceiver calibration	Transceiver Calibration	100	—	125	MHz

(38) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

Symbol/Description	Condition	Transceiver Speed Grades 1, 2, 3, 4, and 5			Unit
		Min	Typ	Max	
`reconfig_clk`	Reconfiguration interface	100	—	125	MHz

Table 32: Transceiver Clock Network Maximum Data Rate Specifications

Clock Network	Maximum Performance			Channel Span	Unit
	ATX [39]	fPLL	CMU		
x1	17.4	12.5	10.3125	6 channels	Gbps
x6	17.4	12.5	N/A	6 channels	Gbps
x6 PLL feedback	17.4	12.5	N/A	Side-wide	Gbps
xN at 0.95 V	10.5	10.5	N/A	Up two banks and down two banks	Gbps
xN at 1.03 V	15.0	12.5	N/A	Up two banks and down two banks	Gbps
xN at 1.12 V	16.0	12.5	N/A	Up two banks and down two banks	Gbps

Table 33: Receiver Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grades 1, 2, 3, 4, and 5			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O, CML, Differential LVPECL, and LVDS			
Absolute V_{MAX} for a receiver pin [40]	—	—	—	1.2	V

(39) ATX maximum data rate support per speed grade.

Symbol/Description	Condition	Transceiver Speed Grades 1, 2, 3, 4, and 5			Unit
		Min	Typ	Max	
Absolute V_{MIN} for a receiver pin [40]	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration [41]	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration [41]	V_{CCR_GXB} = 1.12 V	—	—	2.0	V
	V_{CCR_GXB} = 1.03 V	—	—	2.0	V
	V_{CCR_GXB} = 0.95 V	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins [42]	—	50	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85 ± 30%	—	Ω
	100-Ω setting	—	100 ± 30%	—	Ω

(40) The device cannot tolerate prolonged operation at this absolute maximum.
(41) DC coupling specifications are pending silicon characterization.
(42) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

Symbol/Description	Condition	Transceiver Speed Grades 1, 2, 3, 4, and 5			Unit
		Min	Typ	Max	
V_{ICM} (AC and DC coupled)	V_{CCR_GXB} = 0.95 V	—	600	—	mV
	V_{CCR_GXB} = 1.03 V	—	700	—	mV
	V_{CCR_GXB} = 1.12 V	—	700	—	mV
t_{LTR} (43)	—	—	—	10	µs
t_{LTD} (44)	—	4	—	—	µs
t_{LTD_manual} (45)	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ (46)	—	15	—	—	µs
Run Length	—	—	—	200	UI
CDR PPM tolerance	PCIe-only	-300	—	300	PPM
	All other protocols	-1000	—	1000	PPM
Programmable DC Gain	DC Gain Setting = 0	—	-10	—	dB
	DC Gain Setting = 1	—	-6.5	—	dB
	DC Gain Setting = 2	—	-3	—	dB
	DC Gain Setting = 3	—	0.5	—	dB
	DC Gain Setting = 4	—	4	—	dB

(43) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
(44) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.
(45) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.
(46) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

Table 34: Transmitter Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grades 1, 2, 3, 4, and 5			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O (47)			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
	120-Ω setting	—	120 ± 20%	—	Ω
	150-Ω setting	—	150 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT} = 0.95 V	—	450	—	mV
	V_{CCT} = 1.03 V	—	500	—	mV
	V_{CCT} = 1.12 V	—	550	—	mV
V_{OCM} (DC coupled)	V_{CCT} = 0.95 V	—	450	—	mV
	V_{CCT} = 1.03 V	—	500	—	mV
	V_{CCT} = 1.12 V	—	550	—	mV
Rise time (48)	20% to 80%	20	—	130	ps
Fall time (48)	80% to 20%	20	—	130	ps
Intra-differential pair skew(49)	TX V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15	ps

(47) High Speed Differential I/O is the dedicated I/O standard for the transmitter in Arria 10 transceivers.
(48) The Quartus Prime software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
(49) In QPI mode, if V_{CM} < 0.17 V, the input Vid must be greater than 100 mV. If V_{CM} > 0.17 V, the input Vid must be greater than 70 mV.

Table 35: Typical Transmitter V_{OD} Settings—Preliminary

Symbol	V_{OD} Setting	V_{OD}/V_{CCT} Ratio
V_{OD} differential value = V_{OD}/V_{CCT} ratio x V_{CCT}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70
	21	0.67
	20	0.63
	19	0.60
	18	0.57
	17	0.53
	16	0.50
	15	0.47
	14	0.43
	13	0.40
	12	0.37

Core Performance Specifications

Clock Tree Specifications

Table 36: Clock Tree Performance for Arria 10 Devices—Preliminary

Parameter	Performance			Unit
	–E1L,–E1M [50], –E1S, –I1L, –I1M [50], –I1S	–E2L, –E2S, –I2L, –I2S	–E1M [51], –I1M [51], –E3S, –I3S	
Global clock, regional clock, and small periphery clock	644	644	644	MHz
Large periphery clock	525	525	525	MHz

PLL Specifications

Fractional PLL Specifications

Table 37: Fractional PLL Specifications for Arria 10 Devices—Preliminary

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	—	30	—	800	MHz
f_{INPFD}	Input clock frequency to the phase frequency detector (PFD)	—	30	—	700	MHz
f_{VCO}	PLL voltage-controlled oscillator (VCO) operating range	—	3.5	—	7.05	GHz
$t_{EINDUTY}$	Input clock duty cycle	—	45	—	55	%

(50) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.
(51) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.
(52) This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OUT}	Output frequency for internal global or regional clock	—	—	—	644	MHz
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `reconfig_clk`	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `pll_powerdown`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	—	—	TBD	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `pll_powerdown` signal	—	10	—	—	ns
t_{INCCJ} (53)(54)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	TBD	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	TBD	ps (p-p)
t_{FOUTPJ} (55)	Period jitter for clock output in fractional mode	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
$t_{FOUTCCJ}$ (55)	Cycle-to-cycle jitter for clock output in fractional mode	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
t_{OUTPJ} (55)	Period jitter for clock output in integer mode	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)

(53) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.
(54) F_{REF} is f_{IN}/N, specification applies when $N = 1$.
(55) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Arria 10 Devices table.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{OUTCCJ} (55)	Cycle-to-cycle jitter for clock output in integer mode	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	—	32	—	bit

Related Information

Memory Output Clock Jitter Specifications on page 58
Provides more information about the external memory interface clock output jitter specifications.

I/O PLL Specifications

Table 38: I/O PLL Specifications for Arria 10 Devices—Preliminary

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–1 speed grade	10	—	800 (56)	MHz
		–2 speed grade	10	—	700 (56)	MHz
		–3 speed grade	10	—	650 (56)	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{VCO}	PLL VCO operating range	–1 speed grade	600	—	1600	MHz
		–2 speed grade	600	—	1434	MHz
		–3 speed grade	600	—	1250	MHz
f_{CLBW}	PLL closed-loop bandwidth	—	0.1	—	8	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (C counter)	–1, –2, –3 speed grade	—	—	644	MHz

(56) This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OUT_EXT}	Output frequency for external clock output	–1 speed grade	—	—	800	MHz
		–2 speed grade	—	—	720	MHz
		–3 speed grade	—	—	650	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	—	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	10	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	—	10	—	—	ns
t_{INCCJ} (57)(58)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	TBD	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	TBD	ps (p-p)
t_{OUTPJ_DC}	Period jitter for dedicated clock output	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
t_{OUTCCJ_DC}	Cycle-to-cycle jitter for dedicated clock output	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)

(57) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(58) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{OUTPJ_IO} (59)	Period jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
t_{OUTCCJ_IO} (59)	Cycle-to-cycle jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$	Period jitter for dedicated clock output in cascaded PLLs	$F_{OUT} \geq 100$ MHz	—	—	TBD	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	TBD	mUI (p-p)

Related Information

Memory Output Clock Jitter Specifications on page 58
Provides more information about the external memory interface clock output jitter specifications.

DSP Block Specifications

Table 39: DSP Block Performance Specifications for Arria 10 Devices (V_{CC} and V_{CCP} at 0.9 V Typical Value)—Preliminary

Mode	Performance						Unit
	–E1L, –E1M (60), –E1S	–I1L, –I1M (60), –I1S	–E2L, –E2S, –E2V	–I2L, –I2S, –I2V	–E1M (61), –E3S, –E3V	–I1M (61), –I3S, –I3V	
Fixed-point 18 × 19 multiplication mode	548	528	456	438	364	346	MHz
Fixed-point 27 × 27 multiplication mode	541	522	450	434	358	344	MHz
Fixed-point 18 × 18 multiplier adder mode	548	529	459	440	370	351	MHz

(59) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Arria 10 Devices table.
(60) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.
(61) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.

Mode	Performance						Unit
	–E1L, –E1M [60], –E1S	–I1L, –I1M [60], –I1S	–E2L, –E2S, –E2V	–I2L, –I2S, –I2V	–E1M [61], –E3S, –E3V	–I1M [61], –I3S, –I3V	
Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode	539	517	444	422	349	326	MHz
Fixed-point 18 × 19 systolic mode	548	529	459	440	370	351	MHz
Complex 18 × 19 multiplication mode	548	528	456	438	364	346	MHz
Floating point multiplication mode	548	527	447	427	347	326	MHz
Floating point adder or substract mode	488	471	388	369	288	266	MHz
Floating point multiplier adder or substract mode	483	465	386	368	290	270	MHz
Floating point multiplier accumulate mode	510	490	418	393	326	294	MHz
Floating point vector one mode	502	482	404	382	306	282	MHz
Floating point vector two mode	474	455	383	367	293	278	MHz

Table 40: DSP Block Performance Specifications for Arria 10 Devices (V_{CC} and V_{CCP} at 0.95 V Typical Value)—Preliminary

Mode	Performance		Unit
	–I1L, –I1M [60], –I1S	–I2L, –I2S	
Fixed-point 18 × 19 multiplication mode	635	517	MHz
Fixed-point 27 × 27 multiplication mode	633	517	MHz
Fixed-point 18 × 18 multiplier adder mode	635	516	MHz
Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode	631	509	MHz
Fixed-point 18 × 19 systolic mode	635	516	MHz

[60] When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.
[61] When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.

Mode	Performance		Unit
	–I1L, –I1M (60), –I1S	–I2L, –I2S	
Complex 18 × 19 multiplication mode	635	517	MHz
Floating point multiplication mode	635	501	MHz
Floating point adder or substract mode	564	468	MHz
Floating point multiplier adder or substract mode	564	475	MHz
Floating point multiplier accumulate mode	581	482	MHz
Floating point vector one mode	574	471	MHz
Floating point vector two mode	550	450	MHz

Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to **50%** output duty cycle. Use the Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 41: Memory Block Performance Specifications for Arria 10 Devices (V_{CC} and V_{CCP} at 0.9 V Typical Value)—Preliminary

Memory	Mode	Performance					
		–E1L, –E1M (62), –E1S	–I1, –I1M (62), –I1S	–E2L, –E2S, –E2V, –I2L, –I2S, –I2V	–E3S, –E1M (63), –E3V	–I1M (63), –I3S, –I3V	Unit
MLAB	Single port, all supported widths (×16/×32)	700	660	570	490	490	MHz
	Simple dual-port, all supported widths (×16/×32)	700	660	570	490	490	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	460	450	400	330	330	MHz
	ROM, all supported width (×16/×32)	700	660	570	490	490	MHz
M20K Block	Single-port, all supported widths	730	690	625	530	510	MHz
	Simple dual-port, all supported widths	730	690	625	530	510	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	550	520	470	410	410	MHz
	Simple dual-port with ECC enabled, 512 × 32	470	450	410	360	360	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	620	590	520	470	470	MHz
	True dual port, all supported widths	730	690	600	480	480	MHz
	ROM, all supported widths	730	690	625	530	510	MHz

(62) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.
(63) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.

Table 42: Memory Block Performance Specifications for Arria 10 Devices (V_{CC} and V_{CCP} at 0.95 V Typical Value)—Preliminary

Memory	Mode	Performance		
		–I1L, –I1M [62], –I1S	–I2L, –I2S	Unit
MLAB	Single port, all supported widths (×16/×32)	706	610	MHz
	Simple dual-port, all supported widths (×16/×32)	706	610	MHz
	Simple dual-port with read and write at the same address	482	428	MHz
	ROM, all supported width (×16/×32)	706	610	MHz
M20K Block	Single-port, all supported widths	735	670	MHz
	Simple dual-port, all supported widths	735	670	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	555	500	MHz
	Simple dual-port with ECC enabled, 512 × 32	480	440	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	630	555	MHz
	True dual port, all supported widths	735	640	MHz
	ROM, all supported widths	735	670	MHz

Temperature Sensing Diode Specifications

Internal Temperature Sensing Diode Specifications

Table 43: Internal Temperature Sensing Diode Specifications for Arria 10 Devices—Preliminary

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution
–40 to 125 °C	±5 °C	No	1 MHz	< 5 ms	10 bits

Related Information

Transfer Function for Internal TSD
Provides the transfer function for the internal TSD.

External Temperature Sensing Diode Specifications

Table 44: External Temperature Sensing Diode Specifications for Arria 10 Devices—Preliminary

- The typical value is at 25°C.
- Diode accuracy improves with lower injection current.
- Absolute accuracy is dependent on third party external diode ADC and integration specifics.

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	10	—	100	µA
V_{bias}, voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	—	1.03	—	—

Internal Voltage Sensor Specifications

Table 45: Internal Voltage Sensor Specifications for Arria 10 Devices—Preliminary

Parameter	Minimum	Typical	Maximum	Unit
Resolution	—	—	6	Bit
Sampling rate	—	—	500	Ksps
Differential non-linearity (DNL)	—	—	±1	LSB
Integral non-linearity (INL)	—	—	±1	LSB
Gain error	—	—	±1	%
Offset error	—	—	±1	LSB
Input capacitance	—	20	—	pF
Clock frequency	0.1	—	11	MHz

Parameter		Minimum	Typical	Maximum	Unit
Unipolar Input Mode	Input signal range for Vsigp	0	—	1.5	V
	Common mode voltage on Vsign	0	—	0.25	V
	Input signal range for Vsigp – Vsign	0	—	1.25	V

Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 46: High-Speed I/O Specifications for Arria 10 Devices—Preliminary

When serializer/deserializer (SERDES) factor J = 3 to 10, use the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

Symbol	Condition	–E1L, –E1M (64), –E1S, –I1L, –I1M (64), –I1S			–E2L, –E2S, –I2L, –I2S			–E1M (65), –I1M (65), –E3S, –I3S			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (66)	10	—	800	10	—	700	10	—	625	MHz

(64) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.
(65) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.
(66) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

Symbol	Condition	–E1L, –E1M (64), –E1S, –I1L, –I1M (64), –I1S			–E2L, –E2S, –I2L, –I2S			–E1M (65), –I1M (65), –E3S, –I3S			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 (66)	10	—	625	10	—	625	10	—	525	MHz
f_{HSCLK_OUT} (output clock frequency)	—	—	—	800 (67)	—	—	700 (67)	—	—	625 (67)	MHz

(64) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.
(65) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.
(67) This is achieved by using the PHY clock network.

Symbol		Condition	–E1L, –E1M (64), –E1S, –I1L, –I1M (64), –I1S			–E2L, –E2S, –I2L, –I2S			–E1M (65), –I1M (65), –E3S, –I3S			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate) (68)	SERDES factor J = 4 to 10 (69)(71)(70)	(71)	—	1600 (72)	(71)	—	1434 (72)	(71)	—	1250 (72)	Mbps
		SERDES factor J = 3 (69)(71)(70)	(71)	—	(72)	(71)	—	(72)	(71)	—	(72)	Mbps
		SERDES factor J = 2, uses DDR registers	(71)	—	333 (73)	(71)	—	275 (73)	(71)	—	250 (73)	Mbps
		SERDES factor J = 1, uses DDR registers	(71)	—	333 (73)	(71)	—	275 (73)	(71)	—	250 (73)	Mbps
	$t_{x\ Jitter}$ - True Differential I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	—	—	160	—	—	200	—	—	250	ps
		Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.12	—	—	0.15	UI
	t_{DUTY} (74)	TX output clock duty cycle for Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
	t_{RISE} & & t_{FALL} (70)(75)	True Differential I/O Standards	—	—	160	—	—	180	—	—	200	ps
	TCCS (74)(68)	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps

(64) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.
(65) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.

Symbol		Condition	–E1L, –E1M (64), –E1S, –I1L, –I1M (64), –I1S			–E2L, –E2S, –I2L, –I2S			–E1M (65), –I1M (65), –E3S, –I3S			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10 (69)(71)(70)	—	—	1600	—	—	1434	—	—	1250	Mbps
		SERDES factor J = 3 (69)(71)(70)	—	—	(72)	—	—	(72)	—	—	(72)	Mbps
	f_{HSDR} (data rate) (without DPA) (68)	SERDES factor J = 3 to 10	(71)	—	(76)	(71)	—	(76)	(71)	—	(76)	Mbps
		SERDES factor J = 2, uses DDR registers	(71)	—	(73)	(71)	—	(73)	(71)	—	(73)	Mbps
		SERDES factor J = 1, uses DDR registers	(71)	—	(73)	(71)	—	(73)	(71)	—	(73)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI

(68) Requires package skew compensation with PCB trace length.

(69) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(70) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(71) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

(72) Pending silicon characterization.

(73) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.

(74) Not applicable for `DIVCLK` = 1.

(75) This applies to default pre-emphasis and V_{OD} settings only.

Symbol		Condition	–E1L, –E1M [64], –E1S, –I1L, –I1M [64], –I1S			–E2L, –E2S, –I2L, –I2S			–E1M [65], –I1M [65], –E3S, –I3S			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	± ppm
Non DPA mode	Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

DPA Lock Time Specifications

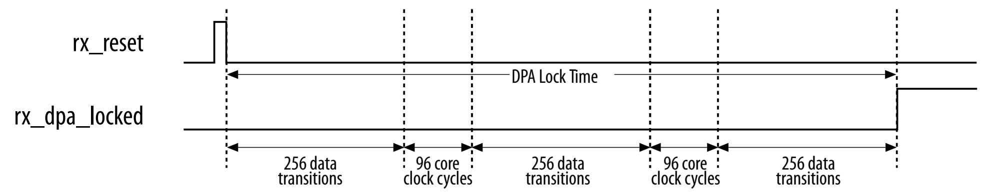


Figure 2: DPA Lock Time Specifications with DPA PLL Calibration Enabled

(64) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.
(65) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.
(76) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.
(64) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.
(65) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.

Table 47: DPA Lock Time Specifications for Arria 10 Devices—Preliminary

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (77)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

(77) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 3: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps

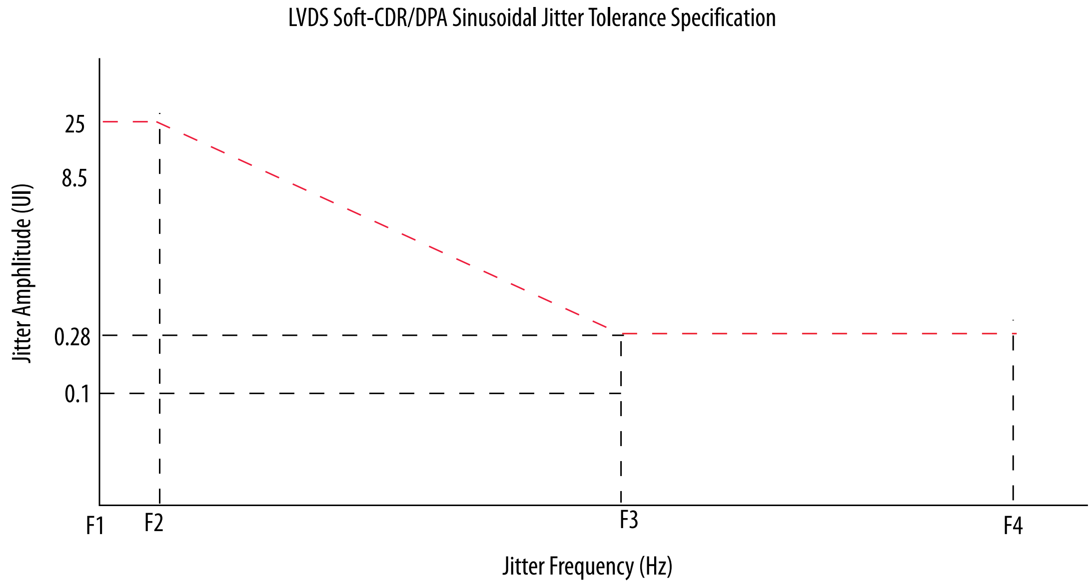
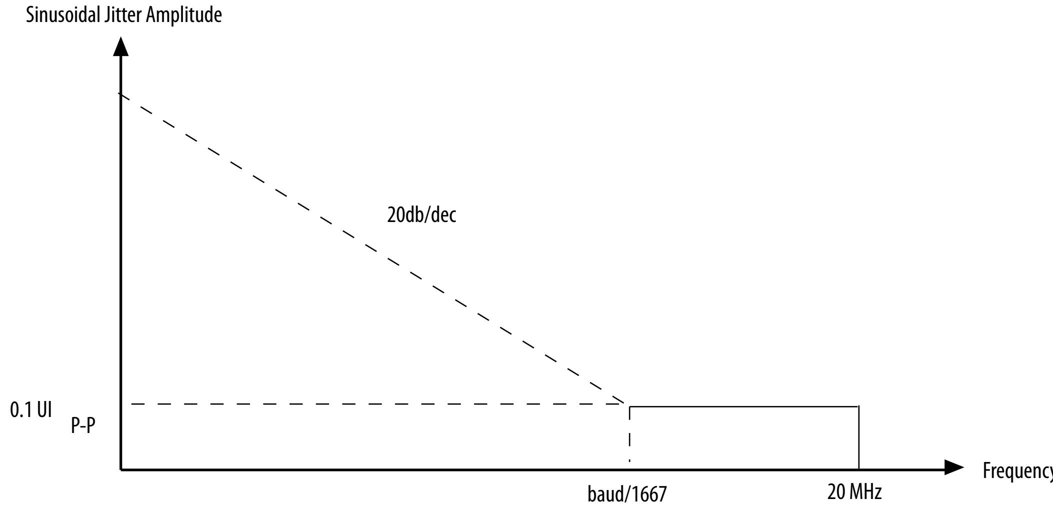


Table 48: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps—Preliminary

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.00
F2	17,565	25.00
F3	1,493,000	0.28
F4	50,000,000	0.28

Figure 4: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.6 Gbps



Memory Standards Supported by the Hard Memory Controller

Table 49: Memory Standards Supported by the Hard Memory Controller for Arria 10 Devices—Preliminary

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				LVDS I/O Bank	3 V I/O Bank
DDR4 SDRAM	Quarter rate	–1	Yes	1,067	—
			—	1,333	—
		–2	Yes	933	—
			—	1,067	—
		–3	Yes	800	—
			—	933	—

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				LVDS I/O Bank	3 V I/O Bank
DDR3 SDRAM	Half rate	–1	Yes	467	467
			—	533	533
		–2	Yes	467	450
			—	533	450
		–3	Yes	400	333
			—	533	333
	Quarter rate	–1	Yes	933	533
			—	1,067	533
		–2	Yes	933	450
			—	1,067	450
		–3	Yes	800	333
			—	933	333

Memory Standard	Rate Support	Speed Grade	Ping Pong PHY Support	Maximum Frequency (MHz)	
				LVDS I/O Bank	3 V I/O Bank
DDR3L SDRAM	Half rate	–1	Yes	467	467
			—	533	533
		–2	Yes	467	450
			—	533	450
		–3	Yes	400	333
			—	533	333
	Quarter rate	–1	Yes	933	533
			—	1,067	533
		–2	Yes	833	450
			—	1,067	450
		–3	Yes	800	333
			—	933	333
LPDDR3 SDRAM	Half rate	–1	—	400	400
		–2	—	400	400
		–3	—	333	333
	Quarter rate	–1	—	800	533
		–2	—	800	450
		–3	—	667	333

Related Information

External Memory Interface Spec Estimator

Provides the specific details of the memory standards supported.

Memory Standards Supported by the Soft Memory Controller

Table 50: Memory Standards Supported by the Soft Memory Controller for Arria 10 Devices—Preliminary

This table lists the overall capability of the soft memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

Memory Standard	Rate Support	Speed Grade	Maximum Frequency (MHz)	
			LVDS I/O Bank	3 V I/O Bank
RLDRAM 3	Quarter rate	–1	1,200	533
		–2	1,066	450
		–3	933	333
QDR IV SRAM	Quarter rate	–1	1,066	533
		–2	1,066	450
		–3	933	333
QDR II/II+/II+ Xtreme SRAM	Full rate	–1	333	333
		–2	333	333
		–3	333	333
	Half rate	–1	633	533
		–2	550	450
		–3	500	333

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

(78) Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

DLL Range Specifications

Table 51: DLL Frequency Range Specifications for Arria 10 Devices—Preliminary

Arria 10 devices support memory interface frequencies lower than 667 MHz, although the reference clock that feeds the DLL must be at least 667 MHz. To support interfaces below 667 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range.

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	667 – 1333	MHz

DQS Logic Block Specifications

Table 52: DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria 10 Devices—Preliminary

This error specification is the absolute maximum and minimum error.

Symbol	Performance (for All Speed Grades)	Unit
t_{DQS_PSERR}	5	ps

Memory Output Clock Jitter Specifications

Table 53: Memory Output Clock Jitter Specifications for Arria 10 Devices—Preliminary

The clock jitter specification applies to the memory output clock pins clocked by an integer PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Altera recommends using PHY clock networks for better jitter performance.

The memory output clock jitter is applicable when an input jitter of 10 ps peak-to-peak is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

Parameter	Clock Network	Symbol	–E1L, –E1M (79), –E1S, –I1L, –I1M (79), –I1S		–E2L, –E2S, –I2L, –I2S		–E1M (80), –I1M (80), –E3S, –I3S		Unit
			Min	Max	Min	Max	Min	Max	
PHY clock	Clock period jitter	$t_{JIT(per)}$	58	58	58	58	58	58	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	58	58	58	58	58	58	ps
	Duty cycle jitter	$t_{JIT(duty)}$	58	58	58	58	58	58	ps

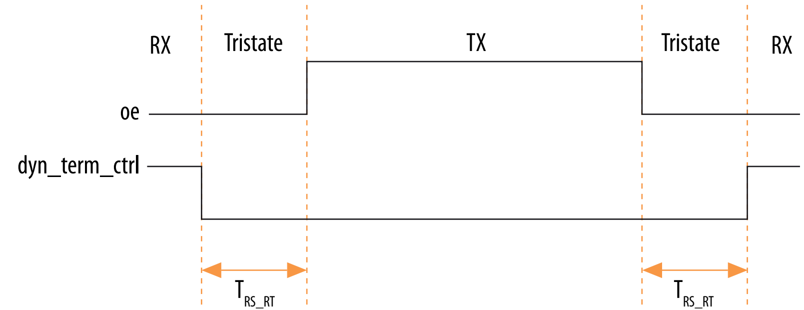
OCT Calibration Block Specifications

Table 54: OCT Calibration Block Specifications for Arria 10 Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT / R_T OCT calibration	> 2000	—	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

(79) When you power V_{CC} and V_{CCP} at nominal voltage of 0.90 V.
(80) When you power V_{CC} and V_{CCP} at lower voltage of 0.83 V.

Figure 5: Timing Diagram for on oe and dyn_term_ctrl Signals



HPS Specifications

This section provides HPS specifications and timing for Arria 10 devices. The specifications are preliminary.

HPS Reset Input Requirements

Table 55: HPS Reset Input Requirements for Arria 10 Devices—Preliminary

Description	Min	Max	Unit
HPS cold reset pulse width	600	—	ns
HPS warm reset pulse width	600	—	ns
Cold reset deassertion to BSEL sampling, using osc1 clock	—	1000	osc1 clocks
Cold reset deassertion to BSEL sampling, using secure clock, without RAM clearing	—	100	µs
Cold reset deassertion to BSEL sampling, using secure clock, with RAM clearing	—	50	ms

HPS Clock Performance

Table 56: HPS Clock Performance for Arria 10 Devices—Preliminary

Symbol/Description	–3 Speed Grade	–2 Speed Grade	–1 Speed Grade	Unit
mpu_base_clk	800	1200	1500	MHz
noc_base_clk	400	400	500	MHz
h2f_user0_clk	400	400	400	MHz
h2f_user1_clk	400	400	400	MHz
hmc_free_clk	433	533	533	MHz

HPS PLL Specifications

HPS PLL Input Requirements

Table 57: HPS PLL Input Requirements for Arria 10 Devices—Preliminary

Description	Min	Typ	Max	Unit
Clock input range	10	—	50	MHz
Clock input jitter tolerance	—	—	2	%
Clock input duty cycle	45	50	55	%

HPS PLL Performance

Table 58: HPS PLL Performance for Arria 10 Devices—Preliminary

Description	–3 Speed Grade		–2 Speed Grade		–1 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
HPS PLL VCO output	320	1600	320	2400	320	3000	MHz

HPS PLL Output Specifications

The maximum HPS PLL lock time is 10 µs for all speed grades.

Quad SPI Flash Timing Characteristics

Table 59: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria 10 Devices—Preliminary

The input parameters are still pending characterization. Note that the Arria 10 HPS boot loader calibrates the input timing automatically.

Symbol	Description	Min	Typ	Max	Unit
T_{qspi_clk}	QSPI_CLK clock period (internal reference clock)	2.5	—	—	ns
T_{clk}	SCLK_OUT clock period (external clock)	10	—	—	ns
$T_{dutycycle}$	SCLK_OUT duty cycle	45	50	55	%
$T_{dssfrst}$[81]	QSPI_SS asserted to first SCLK_OUT edge	0.5	—	3	ns
T_{dsslst}[81]	Last SCLK_OUT edge to QSPI_SS deasserted	–2	—	0.5	ns
T_{do}	QSPI_DATA output delay	1	—	3	ns
T_{din_start}	Valid input data start from falling clock edge	—	—	$[(2 + R_{delay}) \times T_{qspi\_clk}] - 4$	ns
T_{din_end}	Valid input data end from falling clock edge	$[(2 + R_{delay}) \times T_{qspi\_clk}] + 2.2$	—	—	ns
T_{dssb2b}[82]	Minimum delay of slave select deassertion between two back-to-back transfer	1	—	—	SCLK_OUT

(81) You can increase this delay using the delay register in the Quad SPI module.
(82) This delay is programmable in whole QSPI_CLK increments using the delay register in the Quad SPI module.

Figure 6: Quad SPI Flash Serial Output Timing Diagram

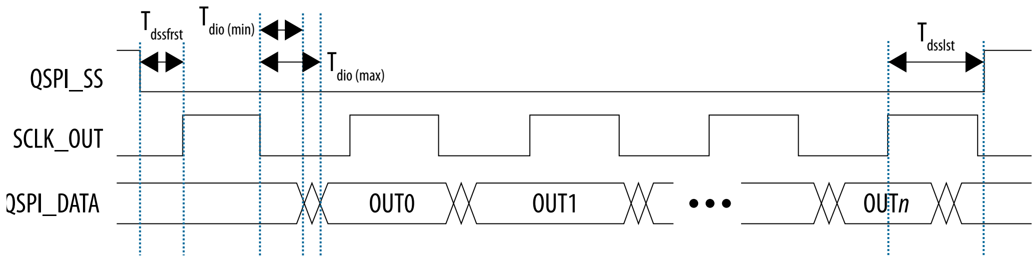
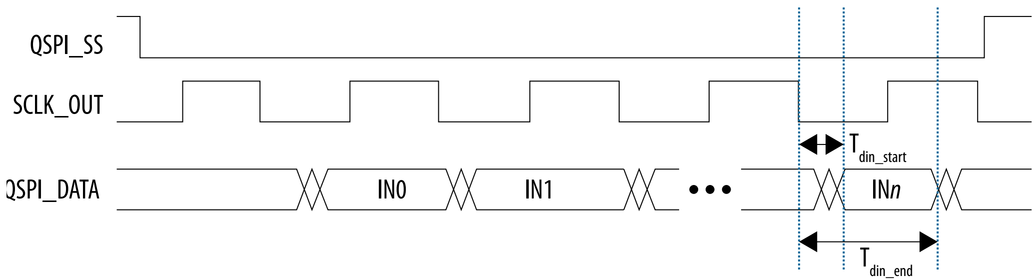


Figure 7: Quad SPI Flash Serial Input Timing Diagram



SPI Timing Characteristics

Table 60: SPI Master Timing Requirements for Arria 10 Devices—Preliminary

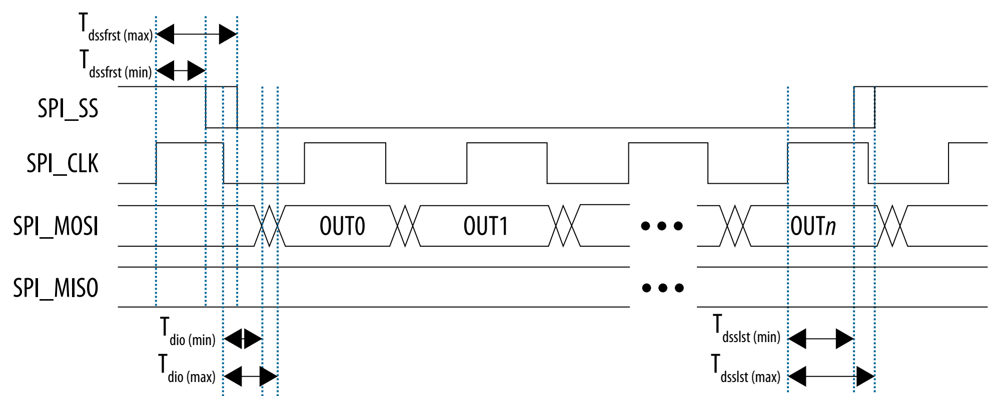
You can adjust the input delay timing using the `rx_sample_dly` register.

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	SPI_CLK clock period	16.67	—	—	ns
$T_{dutycycle}$	SPI_CLK duty cycle	45	50	55	%
$T_{dssfrst}$ (83)	SPI_SS asserted to first SPI_CLK edge	1.5	—	3.5	ns

(83) SPI_SS behavior differs depending on Motorola SPI, TI SSP or Microwire operational mode.

Symbol	Description	Min	Typ	Max	Unit
T_{dsslst} (83)	Last SPI_CLK edge to SPI_SS deasserted	–0.6	—	1.4	ns
T_{dio}	Master-out slave-in (MOSI) output delay	1	—	4	ns
T_{su} (84)	Input setup in respect to SPI_CLK capture edge	2	—	—	ns
T_h (84)	Input hold in respect to SPI_CLK capture edge	0	—	—	ns
T_{dssb2b}	Minimum delay of slave select deassertion between two back-to-back transfers (frames)	1	—	—	SPI_CLK

Figure 8: SPI Master Output Timing Diagram



(84) The capture edge differs depending on the operational mode. For Motorola SPI, the capture edge can be the rising or falling edge depending on the `scpol` register bit; for TI SSP, the capture edge is the falling edge; for Microwire, the capture edge is the rising edge.

Figure 9: SPI Master Input Timing Diagram

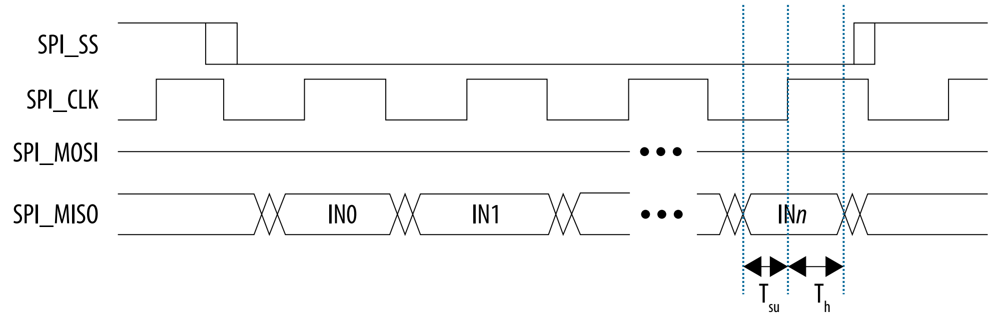


Table 61: SPI Slave Timing Requirements for Arria 10 Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	SPI_CLK clock period	20	—	—	ns
$T_{dutycycle}$	SPI_CLK duty cycle	45	50	55	%
T_s	SPI slave input setup time	5	—	—	ns
T_h	SPI slave input hold time	5	—	—	ns
T_{ssfsu}	SPI_SS asserted to first active SPI_CLK edge setup [85]	5	—	—	ns
T_{ssfh}	SPI_SS asserted to first active SPI_CLK edge hold [85]	5	—	—	ns
T_{sslsu}	SPI_SS deasserted to last active SPI_CLK edge setup [85]	5	—	—	ns
T_{sslh}	SPI_SS deasserted to last active SPI_CLK edge hold [85]	5	—	—	ns
T_d	Master-in slave-out (MISO) output delay	1	—	4	ns

(85) The active edge differs depending on the operational mode. For Motorola SPI, the active edge can be the rising or falling edge depending on the `scpol` register bit; for TI SSP, the active edge is the falling edge; for Microwire, the active edge is the rising edge.

Figure 10: SPI Slave Output Timing Diagram

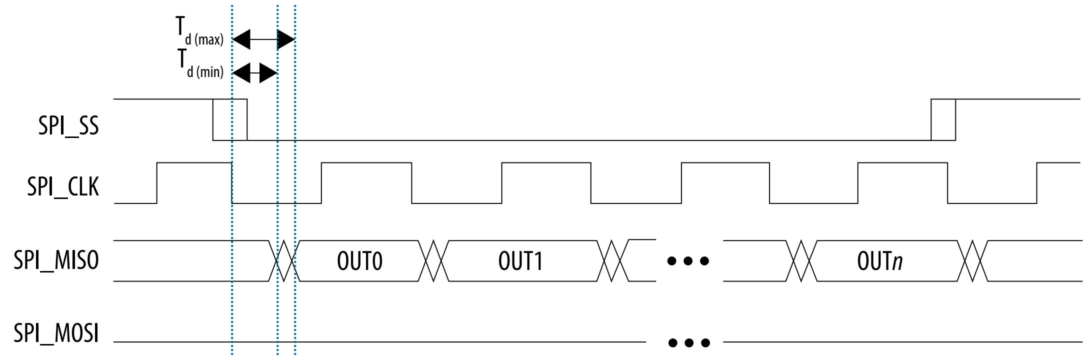
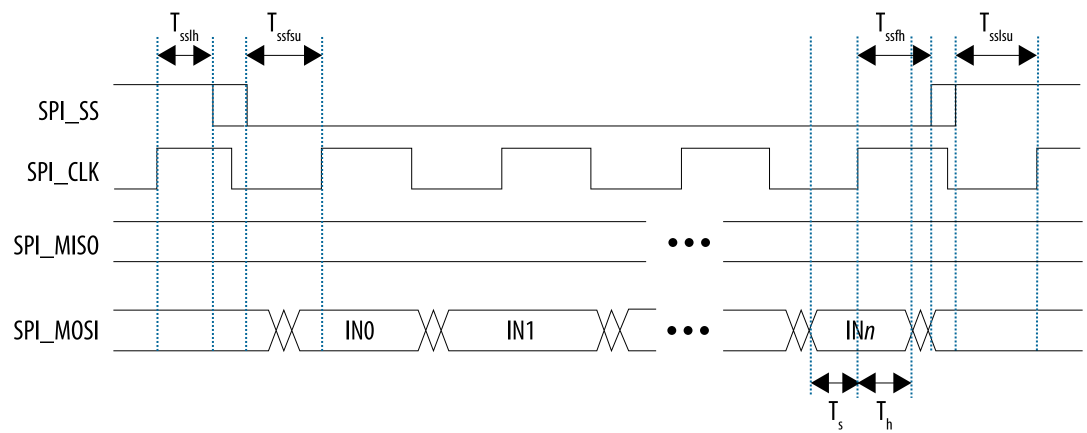


Figure 11: SPI Slave Input Timing Diagram



SD/MMC Timing Characteristics

Table 62: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria 10 Devices—Preliminary

These timings apply to SD, MMC, and embedded MMC cards operating at 1.8 V and 3.3 V.

Symbol	Description	Min	Typ	Max	Unit
$T_{sdmmc\_clk\_out}$	SDMMC_CLK_OUT clock period (Identification mode)	—	2500	—	ns
	SDMMC_CLK_OUT clock period (Standard SD mode)	—	40	—	ns
	SDMMC_CLK_OUT clock period (High speed SD mode)	—	20	—	ns
$T_{dutycycle}$	SDMMC_CLK_OUT duty cycle	45	50	55	%
T_{su}	SDMMC_CMD/SDMMC_D[7:0] input setup [86]	4.0	—	—	ns
T_h	SDMMC_CMD/SDMMC_D[7:0] input hold [87]	1.0	—	—	ns
T_d	SDMMC_CMD/SDMMC_D[7:0] output delay [88]	8.5	—	11.5	ns

(86) These values assume the use of the phase shift implemented in the Boot ROM using `smplsel` = 0 and `TSDMMC_CLK_OUT` = 50 MHz (20 ns) in this equation: 4 – (`TSDMMC_CLK_OUT` × `smpl_sel` / 8) ns. The `smplsel` field is in the `sdmmc` register in the System Manager module.

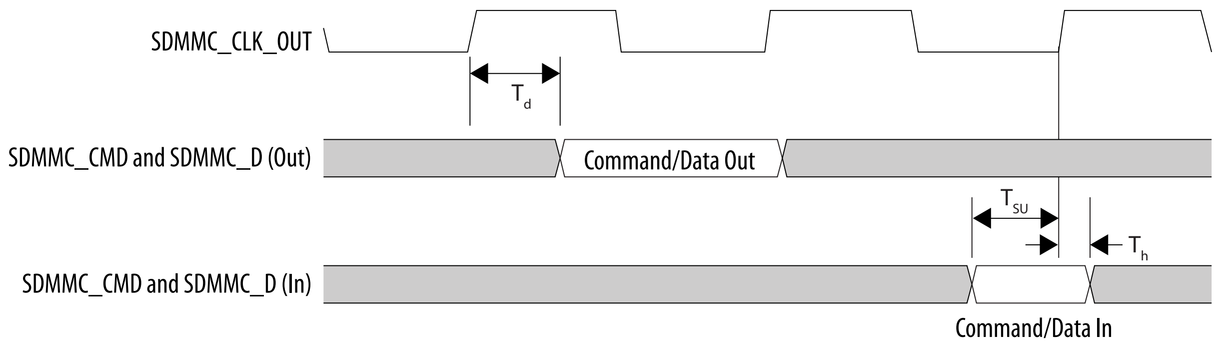
(87) These values assume the use of the phase shift implemented in the Boot ROM using `smplsel` = 0 and `TSDMMC_CLK_OUT` = 50 MHz (20 ns) in this equation: 1 + (`TSDMMC_CLK_OUT` × `smpl_sel` / 8) ns. The `smplsel` field is in the `sdmmc` register in the System Manager module.

(88) These values assume the use of the phase shift implemented in the Boot ROM using `drvsel` = 3 and `TSDMMC_CLK_OUT` = 50 MHz (20 ns) in the following equations:

- For min value: (`TSDMMC_CLK_OUT` × `drv_sel` / 8) + 1 ns
- For max value: (`TSDMMC_CLK_OUT` × `drv_sel` / 8) + 4 ns

The `drvsel` field is in the `sdmmc` register in the System Manager module. You must not set `drvsel` to 0 because this does not provide the necessary delay to meet the hold time of the flash device.

Figure 12: SD/MMC Timing Diagram

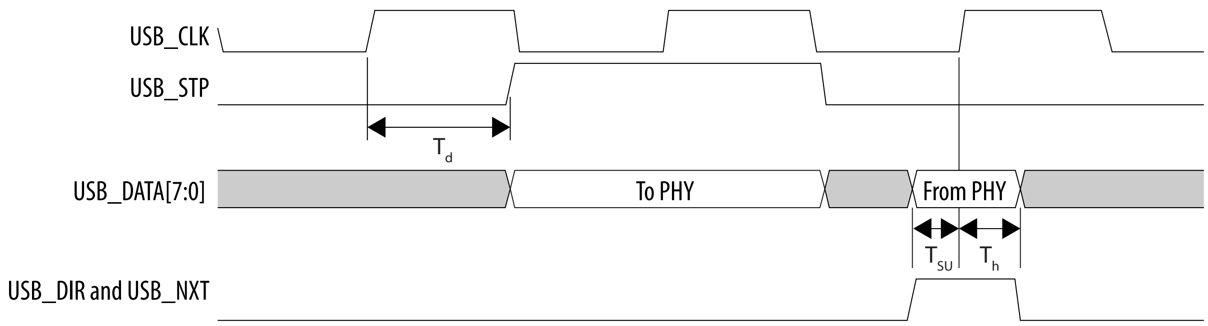


USB ULPI Timing Characteristics

Table 63: USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements for Arria 10 Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	USB_CLK clock period	—	16.667	—	ns
T_d	Clock to USB_STP/USB_DATA[7:0] output delay	1.5	—	8	ns
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	2	—	—	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1	—	—	ns

Figure 13: USB ULPI Timing Diagram



Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 64: Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Arria 10 Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
$T_{dutycycle}$	TX_CLK duty cycle	45	50	55	%
T_d	TX_CLK to TXD/TX_CTL output data delay	–0.5	—	0.5	ns

Figure 14: RGMII TX Timing Diagram

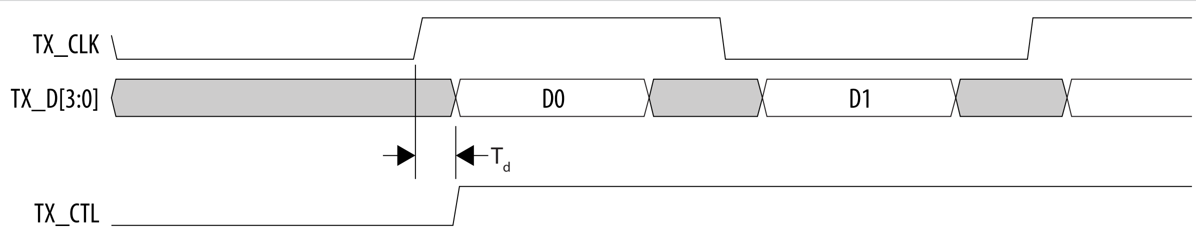


Table 65: RGMII RX Timing Requirements for Arria 10 Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	RX_CLK clock period	—	400	—	ns
T_{su}	RX_D/RX_CTL setup time	1	—	—	ns
T_h	RX_D/RX_CTL hold time	2.5	—	—	ns

Figure 15: RGMII RX Timing Diagram

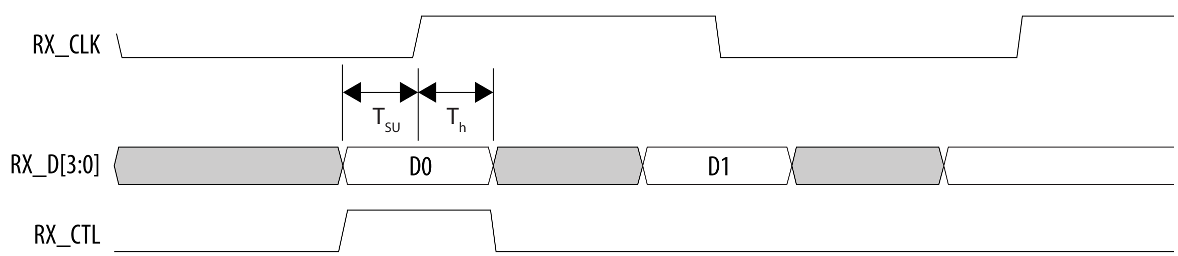


Table 66: Reduced Media Independent Interface (RMII) Clock Timing Requirements for Arria 10 Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (100Base-T)	TX_CLK clock period	—	20	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	20	—	ns
$T_{dutycycle}$	Clock duty cycle, internal clock source	45	50	55	%
$T_{dutycycle}$	Clock duty cycle, external clock source	35	50	65	%

Table 67: RMII TX Timing Requirements for Arria 10 Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
T_d	TX_CLK to TXD/TX_CTL output data delay	0.45	—	4	ns

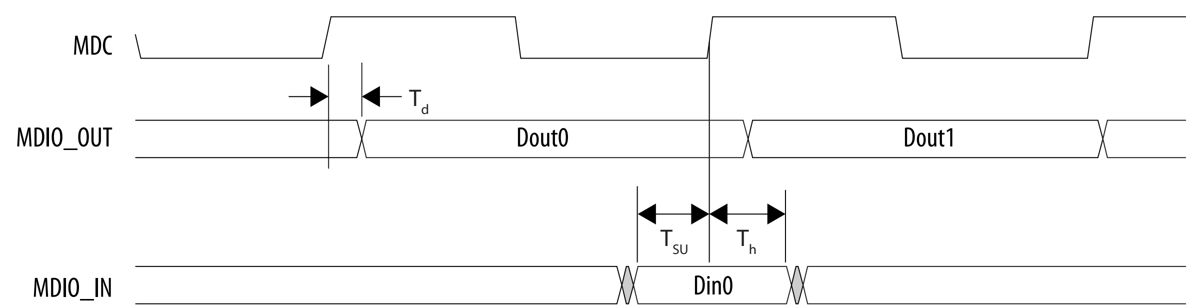
Table 68: RMII RX Timing Requirements for Arria 10 Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
T_{su}	RX_D/RX_CTL setup time	1	—	—	ns
T_h	RX_D/RX_CTL hold time	0.4	—	—	ns

Table 69: Management Data Input/Output (MDIO) Timing Requirements for Arria 10 Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	—	400	—	ns
T_d	MDC to MDIO output data delay	10.2	—	20	ns
T_{su}	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	10	—	—	ns

Figure 16: MDIO Timing Diagram



I^2C Timing Characteristics

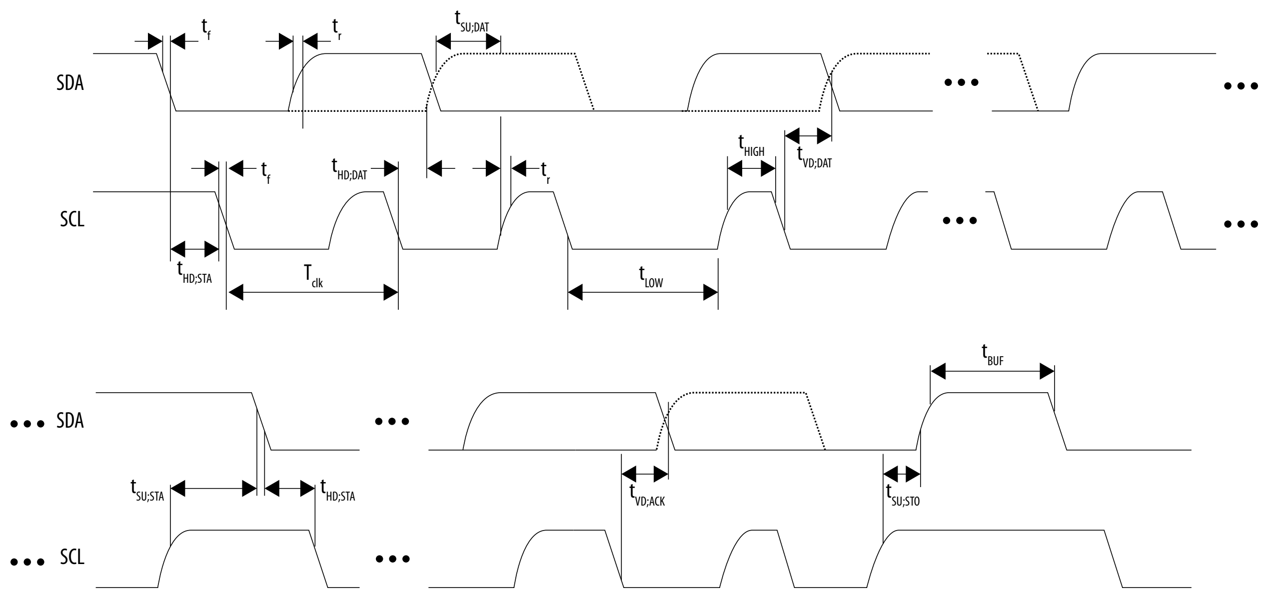
Table 70: I^2C Timing Requirements for Arria 10 Devices—Preliminary

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
t_{HIGH}	SCL high period	4	—	0.6	—	µs
t_{LOW}	SCL low period	4.7	—	1.3	—	µs
$t_{SU;DAT}$	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
$t_{HD;DAT}$ (89)	Hold time for SCL to SDA data	0	3.15	0	0.6	µs
$t_{VD;DAT}$ and $t_{VD;ACK}$	SCL to SDA output data delay	—	3.45	—	0.9	µs
$t_{SU;STA}$	Setup time for a repeated start condition	4.7	—	0.6	—	µs
$t_{HD;STA}$	Hold time for a repeated start condition	4	—	0.6	—	µs
$t_{SU;STO}$	Setup time for a stop condition	4	—	0.6	—	µs
t_{BUF}	SDA high pulse duration between STOP and START	4.7	—	1.3	—	µs
t_r	SCL rise time	—	1000	20	300	ns
t_f	SCL fall time	—	300	$20 \times (V_{dd} / 5.5)$ (90)	300	ns
t_r	SDA rise time	—	1000	20	300	ns
t_f	SDA fall time	—	300	$20 \times (V_{dd} / 5.5)$ (90)	300	ns

(89) You must enable an internal delay in the embedded software. The delay is programmable using the `ic_sda_hold` register in the I^2C controller.

(90) V_{dd} is the I^2C bus voltage.

Figure 17: I²C Timing Diagram



NAND Timing Characteristics

Table 71: NAND ONFI 1.0 Timing Requirements for Arria 10 Devices—Preliminary

Symbol	Description	Min	Max	Unit
t_{WP} [91]	Write enable pulse width	10	—	ns
t_{WH} [91]	Write enable hold time	7	—	ns
t_{RP} [91]	Read enable pulse width	10	—	ns
t_{REH} [91]	Read enable hold time	7	—	ns
t_{CLS} [91]	Command latch enable to write enable setup time	10	—	ns
t_{CLH} [91]	Command latch enable to write enable hold time	5	—	ns
t_{CS} [91]	Chip enable to write enable setup time	15	—	ns
t_{CH} [91]	Chip enable to write enable hold time	5	—	ns
t_{ALS} [91]	Address latch enable to write enable setup time	10	—	ns
t_{ALH} [91]	Address latch enable to write enable hold time	5	—	ns
t_{DS} [91]	Data to write enable setup time	7	—	ns
t_{DH} [91]	Data to write enable hold time	5	—	ns
t_{CEA}	Chip enable to data access time	—	100	ns
t_{REA}	Read enable to data access time	—	40	ns
t_{RHZ}	Read enable to data high impedance	—	200	ns
t_{RR}	Ready to read enable low	20	—	ns
t_{WB} [91]	Write enable high to R/B low	—	200	ns

(91) This timing is software programmable.

Figure 18: NAND Command Latch Timing Diagram

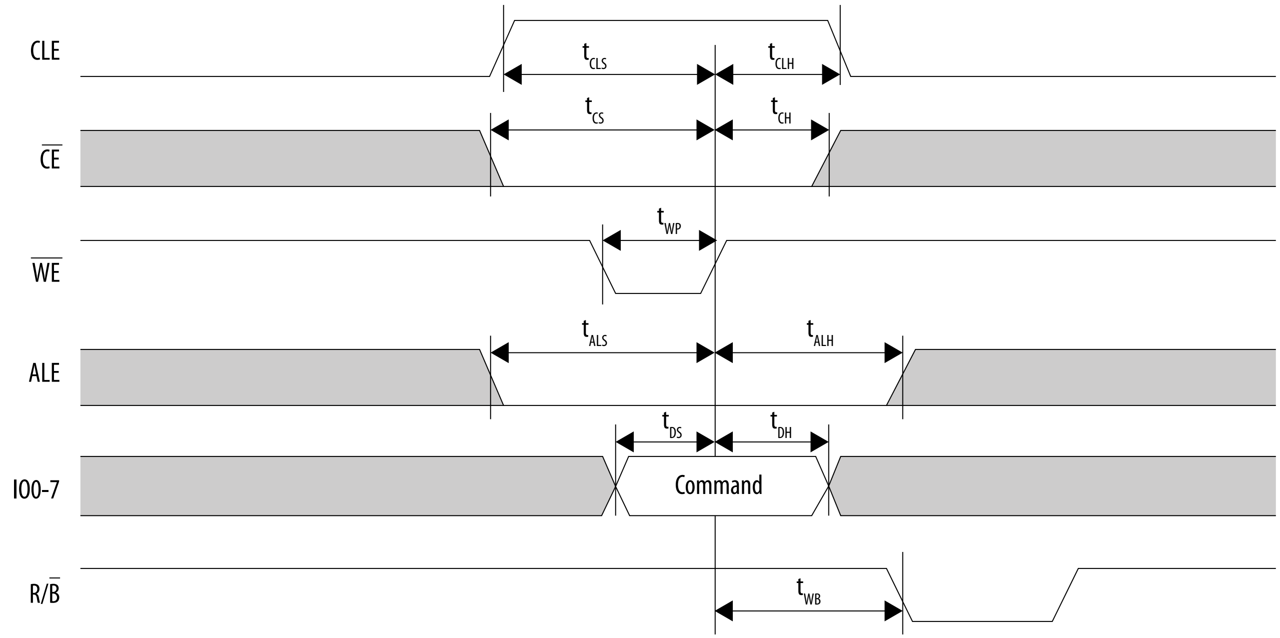


Figure 19: NAND Address Latch Timing Diagram

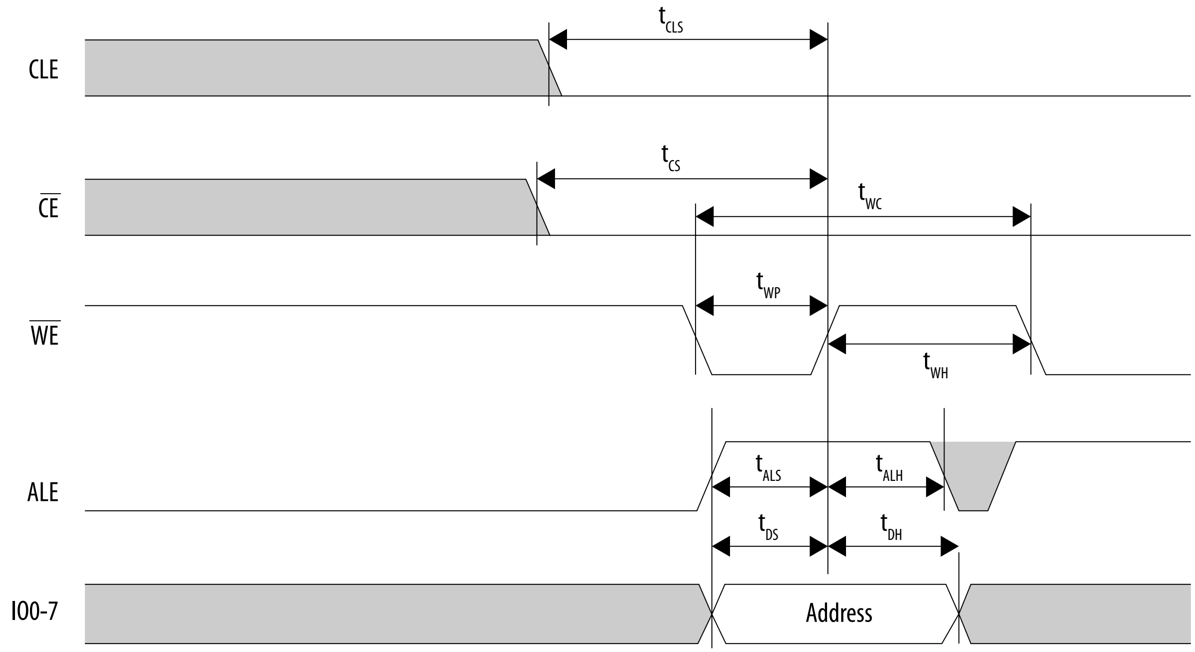


Figure 20: NAND Data Output Cycle Timing Diagram

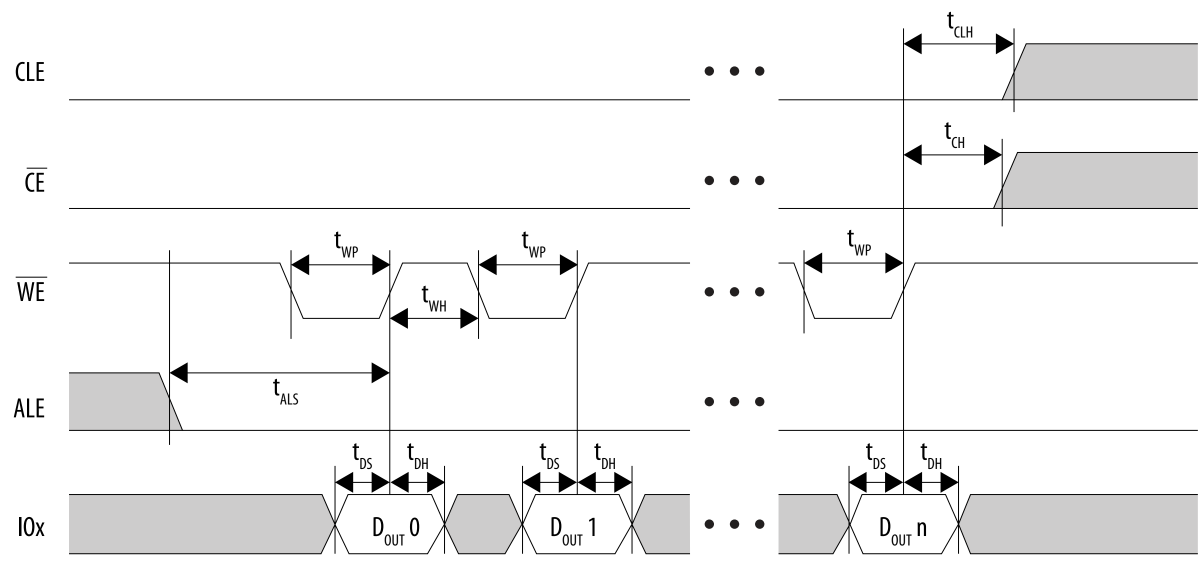


Figure 21: NAND Data Input Cycle Timing Diagram

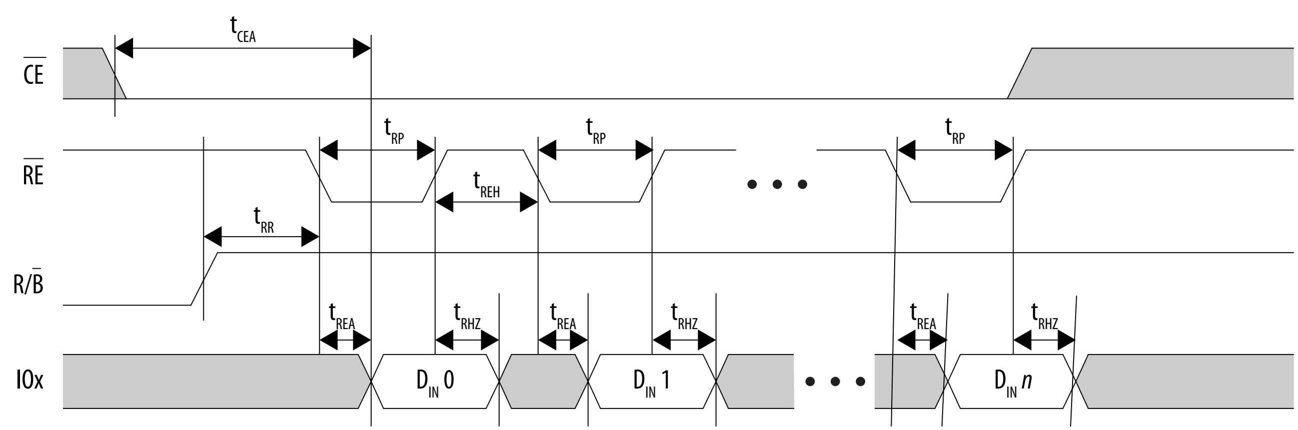


Figure 22: NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle

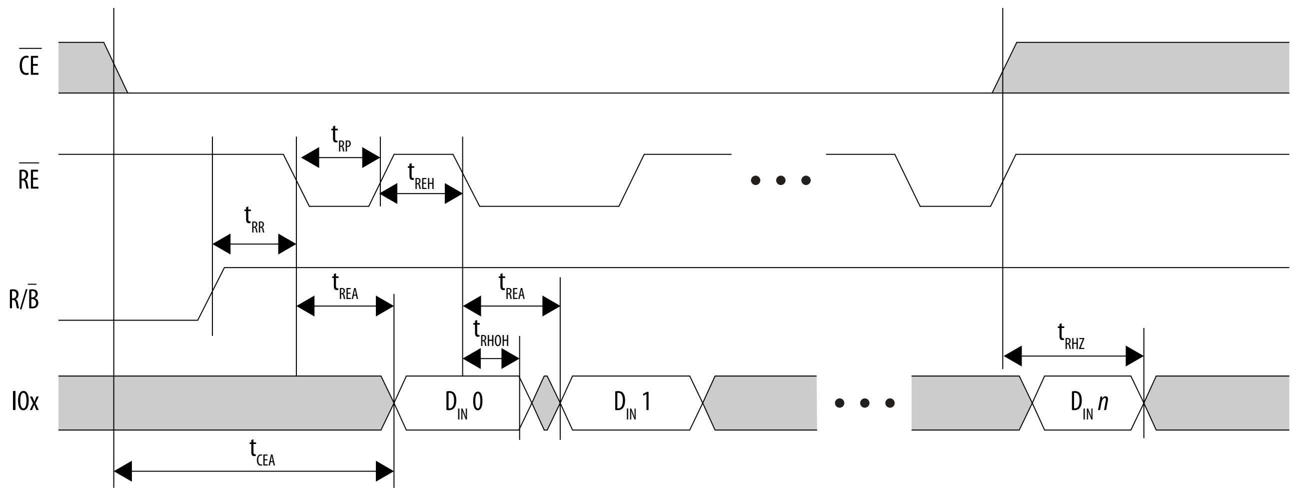


Figure 23: NAND Read Status Timing Diagram

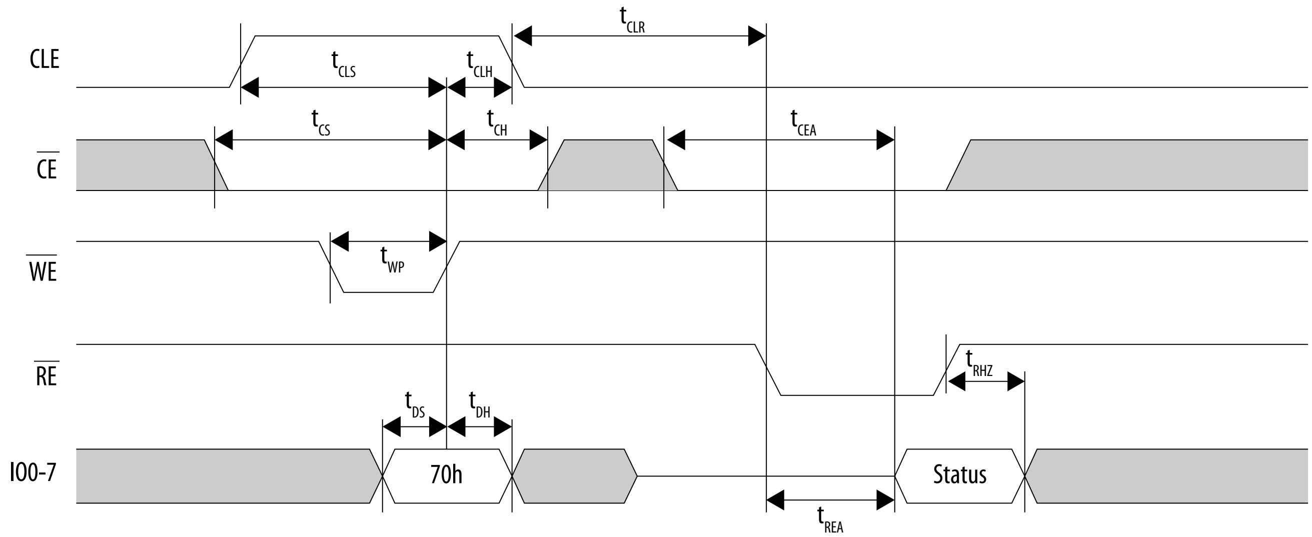
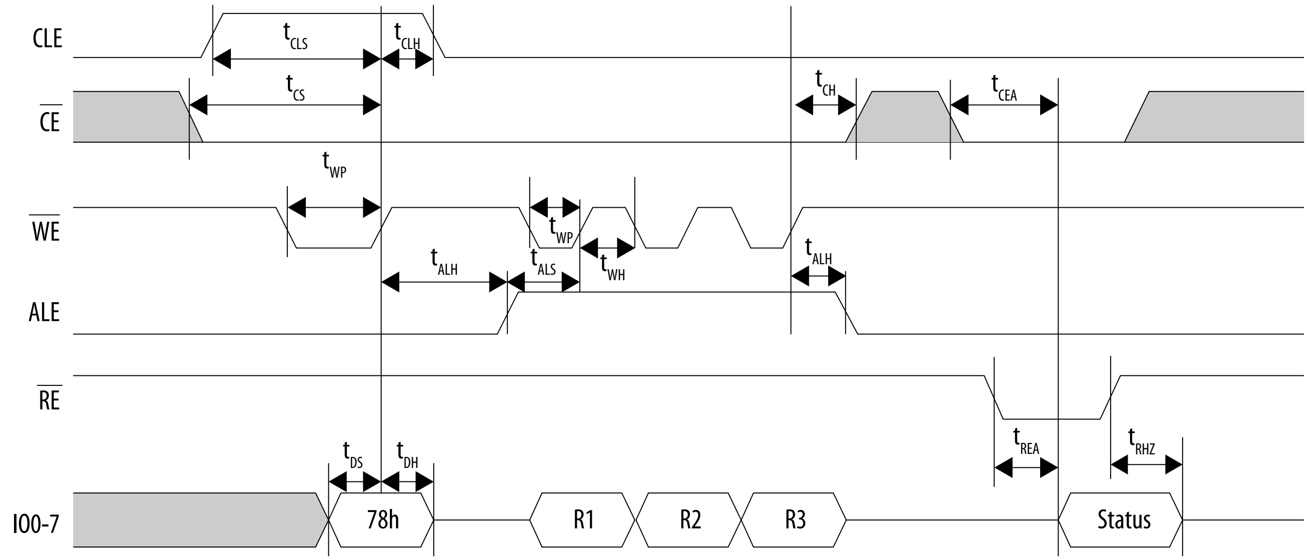


Figure 24: NAND Read Status Enhanced Timing Diagram

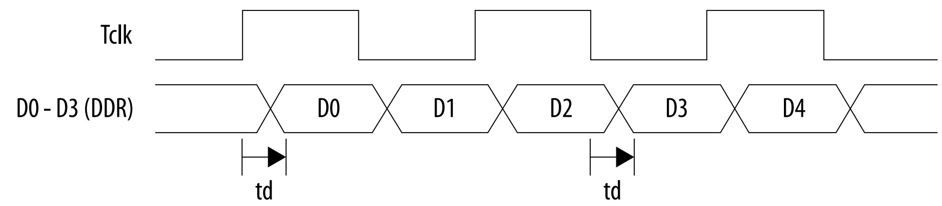


Trace Timing Characteristics

Table 72: Trace Timing Requirements for Arria 10 Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	CLK clock period	5	—	—	ns
$T_{dutycycle}$	CLK maximum duty cycle	45	50	55	%
T_d	CLK to D0–D3 output data delay	–0.5	—	1	ns

Figure 25: Trace Timing Diagram



GPIO Interface

The general-purpose I/O (GPIO) interface has debounce circuitry included to remove signal glitches. The debounce clock frequency ranges from 125 Hz to 32 kHz. The minimum pulse width is 2 debounce clock cycles and the minimum detectable GPIO pulse width is 62.5 us (at 32 kHz). Any pulses shorter than 2 debounce clock cycles are filtered by the GPIO peripheral.

Configuration Specifications

This section provides configuration specifications and timing for Arria 10 devices.

POR Specifications

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

Table 73: Fast and Standard POR Delay Specification for Arria 10 Devices—Preliminary

POR Delay	Minimum	Maximum	Unit
Fast	4	12 [92]	ms
Standard	100	300	ms

[92] The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Related Information

MSEL Pin Settings

Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

JTAG Configuration Timing

Table 74: JTAG Timing Parameters and Values for Arria 10 Devices—Preliminary

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30, 167 [93]	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

(93) The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

Table 75: DCLK-to-DATA[] Ratio for Arria 10 Devices—Preliminary

You cannot turn on encryption and compression at the same time for Arria 10 devices.

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
FPP (32-bit wide)	Off	Off	1
	On	Off	4
	Off	On	8

FPP Configuration Timing when DCLK-to-DATA[] = 1

Note: When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Arria 10 Devices table.

Table 76: FPP Timing Parameters When the DCLK-to-DATA[] Ratio is 1 for Arria 10 Devices—Preliminary

Use these timing parameters when the decompression and design security features are disabled.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 (94)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 (95)	µs

(94) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK} (96)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (96)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16/×32)	—	100	MHz
t_{CD2UM}	CONF_DONE high to user mode (97)	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

(95) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
(96) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(97) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

FPP Configuration Timing when DCLK-to-DATA[] >1

Table 77: FPP Timing Parameters When the DCLK-to-DATA[] Ratio is >1 for Arria 10 Devices—Preliminary

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 [98]	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 [98]	µs
t_{CF2CK} [99]	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} [99]	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N–1/f_{DCLK}$ [100]	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16/×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode [101]	175	830	µs

(98) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(99) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(100) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.
(101) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 78: AS Timing Parameters for AS ×1 and AS ×4 Configurations in Arria 10 Devices—Preliminary

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria 10 Devices table.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	4	ns
t_{SU}	Data setup time before falling edge on DCLK	1	—	ns
t_{DH}	Data hold time after falling edge on DCLK	1.5	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

- PS Configuration Timing on page 86

- **AS Configuration Timing**
  Provides the AS configuration timing waveform.

DCLK Frequency Specification in the AS Configuration Scheme

Table 79: DCLK Frequency Specification in the AS Configuration Scheme—Preliminary

This table lists the internal clock frequency specification for the AS configuration scheme.

The `DCLK` frequency specification applies when you use the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support `DCLK` frequency of 100 MHz.

You can only set 12.5, 25, 50, and 100 MHz in the Quartus Prime software.

Parameter	Minimum	Typical	Maximum	Unit
DCLK frequency in AS configuration scheme	5.3	7.9	12.5	MHz
	10.6	15.7	25.0	MHz
	21.3	31.4	50.0	MHz
	42.6	62.9	100.0	MHz

PS Configuration Timing

Table 80: PS Timing Parameters for Arria 10 Devices—Preliminary

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	`nCONFIG` low to `CONF_DONE` low	—	600	ns
t_{CF2ST0}	`nCONFIG` low to `nSTATUS` low	—	600	ns
t_{CFG}	`nCONFIG` low pulse width	2	—	µs
t_{STATUS}	`nSTATUS` low pulse width	268	3,000 (102)	µs
t_{CF2ST1}	`nCONFIG` high to `nSTATUS` high	—	3,000 (103)	µs

(102) This value is applicable if you do not delay configuration by extending the `nCONFIG` or `nSTATUS` low pulse width.
(103) This value is applicable if you do not delay configuration by externally holding the `nSTATUS` low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK} (104)	nCONFIG high to first rising edge on DCLK	3,010	—	µs
t_{ST2CK} (104)	nSTATUS high to first rising edge of DCLK	10	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (105)	175	830	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (600 × CLKUSR period)	—	—

Related Information

PS Configuration Timing

Provides the PS configuration timing waveform.

Initialization

Table 81: Initialization Clock Source Option and the Maximum Frequency for Arria 10 Devices—Preliminary

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	600
CLKUSR (106)(107)	AS, PS, and FPP	100	

(104) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(105) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

Configuration Files

There are two types of configuration bit stream formats for different configuration schemes:

- PS and FPP—Raw Binary File (**.rbf**)
- AS—Raw Programming Data File (**.rpd**)

The **.rpd** file size follows the Altera configuration devices capacity. However, the actual configuration bit stream size for **.rpd** file is the same as **.rbf** file.

Table 82: Configuration Bit Stream Sizes for Arria 10 Devices—Preliminary

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (**.hex**) or tabular text file (**.ttf**) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus Prime software. However, for a specific version of the Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

Variant	Product Line	Uncompressed Configuration Bit Stream Size (bits)	IOCSR .rbf Size (bits)	Recommended EPCQ-L Serial Configuration Device
Arria 10 GX	GX 016	81,923,582	1,356,716	EPCQ-L256 or higher density
	GX 022	81,923,582	1,356,716	EPCQ-L256 or higher density
	GX 027	122,591,622	1,360,284	EPCQ-L256 or higher density
	GX 032	122,591,622	1,360,284	EPCQ-L256 or higher density
	GX 048	177,341,246	1,454,656	EPCQ-L256 or higher density
	GX 057	252,831,072	1,549,028	EPCQ-L256 or higher density
	GX 066	252,831,072	1,549,028	EPCQ-L256 or higher density
	GX 900	351,292,512	1,885,396	EPCQ-L512 or higher density
	GX 1150	351,292,512	1,885,396	EPCQ-L512 or higher density

(106) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.

(107) If you use the CLKUSR pin for AS and transceiver calibration simultaneously, the only allowed frequency is 100 MHz.

Variant	Product Line	Uncompressed Configuration Bit Stream Size (bits)	IOCSR .rbf Size (bits)	Recommended EPCQ-L Serial Configuration Device
Arria 10 GT	GT 900	351,292,512	1,885,396	EPCQ-L512 or higher density
	GT 1150	351,292,512	1,885,396	EPCQ-L512 or higher density
Arria 10 SX	SX 016	81,923,582	1,356,716	EPCQ-L256 or higher density
	SX 022	81,923,582	1,356,716	EPCQ-L256 or higher density
	SX 027	122,591,622	1,360,284	EPCQ-L256 or higher density
	SX 032	122,591,622	1,360,284	EPCQ-L256 or higher density
	SX 048	177,341,246	1,454,656	EPCQ-L256 or higher density
	SX 057	252,831,072	1,549,028	EPCQ-L256 or higher density
	SX 066	252,831,072	1,549,028	EPCQ-L256 or higher density

Minimum Configuration Time Estimation

Table 83: Minimum Configuration Time Estimation for Arria 10 Devices—Preliminary

The estimated values are based on the uncompressed configuration bit stream sizes in the Configuration Bit Stream Sizes for Arria 10 Devices table.

Variant	Product Line	Active Serial [108]			Fast Passive Parallel [109]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Arria 10 GX	GX 016	4	100	204.81	32	100	25.60
	GX 022	4	100	204.81	32	100	25.60
	GX 027	4	100	306.48	32	100	38.31
	GX 032	4	100	306.48	32	100	38.31
	GX 048	4	100	443.35	32	100	55.42
	GX 057	4	100	632.08	32	100	79.01
	GX 066	4	100	632.08	32	100	79.01
	GX 900	4	100	883.20	32	100	110.40
	GX 1150	4	100	883.20	32	100	110.40
Arria 10 GT	GT 900	4	100	883.20	32	100	110.40
	GT 1150	4	100	883.20	32	100	110.40

(108) The minimum configuration time is calculated based on DCLK frequency of 100 MHz. Only external `CLKUSR` may guarantee the frequency accuracy of 100 MHz. If you use internal oscillator of 100 MHz, you may not get the actual frequency of 100 MHz. For the DCLK frequency using internal oscillator, refer to the DCLK Frequency Specification in the AS Configuration Scheme table.

Variant	Product Line	Active Serial [108]			Fast Passive Parallel [109]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Arria 10 SX	SX 016	4	100	204.81	32	100	25.60
	SX 022	4	100	204.81	32	100	25.60
	SX 027	4	100	306.48	32	100	38.31
	SX 032	4	100	306.48	32	100	38.31
	SX 048	4	100	443.35	32	100	55.42
	SX 057	4	100	632.08	32	100	79.01
	SX 066	4	100	632.08	32	100	79.01

Related Information

- Configuration Files on page 88
- DCLK Frequency Specification in the AS Configuration Scheme on page 86
  Provides the DCLK frequency using internal oscillator.

Remote System Upgrades

Table 84: Remote System Upgrade Circuitry Timing Specifications for Arria 10 Devices—Preliminary

Parameter	Minimum	Maximum	Unit
$f_{MAX\_RU\_CLK}$ [110]	—	40	MHz

(108) The minimum configuration time is calculated based on DCLK frequency of 100 MHz. Only external CLKUSR may guarantee the frequency accuracy of 100 MHz. If you use internal oscillator of 100 MHz, you may not get the actual frequency of 100 MHz. For the DCLK frequency using internal oscillator, refer to the DCLK Frequency Specification in the AS Configuration Scheme table.

(109) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

(109) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

(110) This clock is user-supplied to the remote system upgrade circuitry. If you are using the ALTREMOTE_UPDATE megafunction IP core, the clock user-supplied to the ALTREMOTE_UPDATE IP core must meet this specification.

Parameter	Minimum	Maximum	Unit
$t_{RU\_nCONFIG}$ (111)	250	—	ns
$t_{RU\_nRSTIMER}$ (112)	250	—	ns

Related Information

- **Remote System Upgrade State Machine**
  Provides more information about configuration reset (RU_CONFIG) signal.
- **User Watchdog Timer**
  Provides more information about reset_timer (RU_nRSTIMER) signal.

User Watchdog Internal Circuitry Timing Specifications

Table 85: User Watchdog Internal Oscillator Frequency Specifications for Arria 10 Devices—Preliminary

Parameter	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus Prime Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

Arria 10 I/O Timing Spreadsheet
Provides the Arria 10 Excel-based I/O timing spreadsheet.

(111) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification.
(112) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification.

Programmable IOE Delay

Table 86: IOE Programmable Delay for Arria 10 Devices—Preliminary

For the exact values for each setting, use the latest version of the Quartus Prime software.

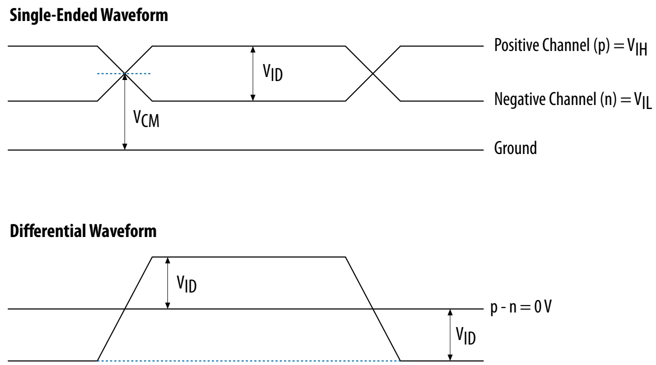
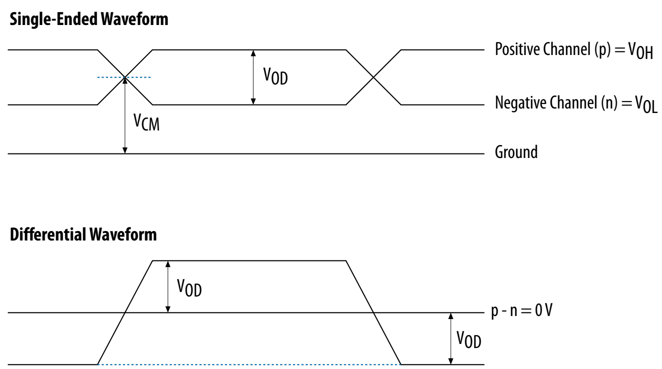
Parameter (113)	Available Settings	Minimum Offset (114)	Fast Model		Slow Model					Unit
			Extended	Industrial	–I1L	–I2S	–I3S	–E2S	–E3S	
Input Delay Chain Setting (IO_IN_DLY_CHN)	64	0	1.829	1.820	4.128	4.764	5.485	4.764	5.485	ns
Output Delay Chain Setting (IO_OUT_DLY_CHN)	16	0	0.433	0.430	0.990	1.145	1.326	1.145	1.326	ns

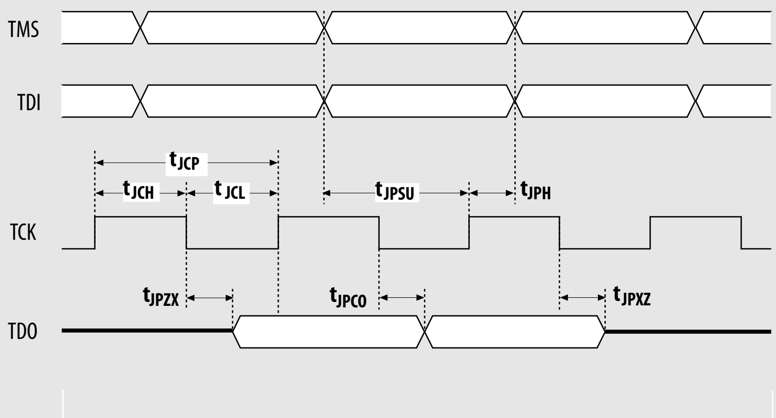
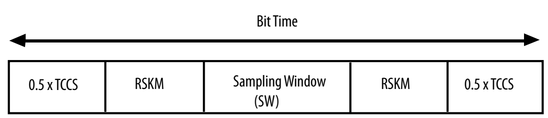
(113) You can set this value in the Quartus Prime software by selecting **Input Delay Chain Setting** or **Output Delay Chain Setting** in the **Assignment Name** column.

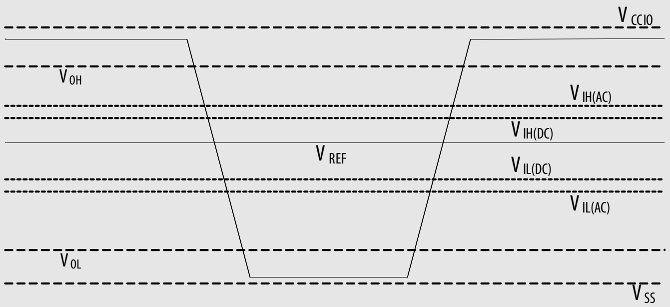
(114) Minimum offset does not include the intrinsic delay.

Glossary

Table 87: Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms  Transmitter Output Waveforms 
f_{HSCLK}	Left/right PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.

Term	Definition
$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications: 
Preliminary	Some tables show the designation as “Preliminary”. Preliminary characteristics are created using simulation results, process data, and other known parameters. Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no preliminary designations on finalized tables.
R_L	Receiver differential input discrete resistor (external to the Arria 10 device).
Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 

Term	Definition
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard 
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
t_{RISE}	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).

Term	Definition
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage
$V_{IH(DC)}$	High-level DC input voltage
V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage
$V_{IL(DC)}$	Low-level DC input voltage
V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
V_{SWING}	Differential input voltage
V_{IX}	Input differential cross point voltage
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock Boost Factor

Document Revision History

Date	Version	Changes
December 2015	2015.12.31	• Updated M20K block specifications for "True dual port, all supported widths" and "ROM, all supported widths" in the Memory Clock Performance Specifications (V_{CC} and V_{CCP} at 0.9 V Typical Value) table. • Updated maximum resolution from 8 bit 6 bit and added minimum clock frequency of 0.1 MHz in Internal Voltage Sensor Specifications for Arria 10 Devices table. • Updated the sinusoidal jitter from 0.35 UI to 0.28 UI in LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications.
December 2015	2015.12.18	• Changed the minimum specifications in the "Transceiver Power Supply Operating Conditions for Arria 10 GT Devices" table. • Changed conditions in the "Transmitter and Receiver Data Rate Performance" table.

November 2015	2015.11.02	• Added power option V which is supported with the SmartVID feature (lowest static power).
		• Added note for SmartVID in Recommended Operating Conditions for Arria 10 Devices table. Note: SmartVID is supported in devices with –2V and –3V speed grades only.
		• Removed 20-Ω R_T in OCT Calibration Accuracy Specifications for Arria 10 Devices table.
		• Updated specifications in OCT Without Calibration Resistance Tolerance Specifications for Arria 10 Devices table.
		• Updated the note for Value column in the Internal Weak Pull-Up Resistor Values for Arria 10 Devices table. Added Internal Weak Pull-Down Resistor Values for Arria 10 Devices table.
		• Updated fractional PLL specifications:
		  • Updated f_{IN} minimum from 50 MHz to 30 MHz and maximum from 1000 MHz to 800 MHz for all speed grades.
		  • Updated f_{INPFD} minimum from 50 MHz to 30 MHz and maximum from 325 MHz to 700 MHz.
		  • Updated f_{VCO} minimum from 3.125 GHz to 3.5 GHz and maximum from 6.25 GHz to 7.05 GHz.
		  • Updated $t_{EINDUTY}$ minimum from 40% to 45% and maximum from 60% to 55%.
		  • Removed the conditions for f_{OUT} and f_{CLBW}.
		  • Updated the descriptions for $f_{DYCONFIGCLK}$, t_{LOCK}, and t_{ARESET}.

Date	Version	Changes

		• Added –E2V, –I2V, –E3V, and –I3V speed grades in DSP Block Performance Specifications for Arria 10 Devices (V_{CC} and V_{CCP} at 0.9 V Typical Value) table.
		• Updated Memory Block Performance Specifications for Arria 10 Devices table for V_{CC} and V_{CCP} at 0.9 V typical value. Added memory block performance specifications for V_{CC} and V_{CCP} at 0.95 V typical value.
		• Removed the "Minimum Resolution with no Missing Codes" column in Internal Temperature Sensing Diode Specifications for Arria 10 Devices table.
		• Added a link in the Internal Temperature Sensing Diode Specifications section: *Transfer Function for Internal TSD* topic in the *Power Management in Arria 10 Devices* chapter, *Arria 10 Core Fabric and General Purpose I/Os Handbook*.
		• Added descriptions to External Temperature Sensing Diode Specifications for Arria 10 Devices table.
		• Updated Internal Voltage Sensor Specifications for Arria 10 Devices table.
		  • Updated maximum resolution from 12 bits to 8 bits. Removed minimum resolution value.
		  • Updated maximum integral non-linearity (INL) from ±3 LSB to ±1 LSB.
		  • Updated maximum clock frequency from 20 MHz to 11 MHz.
		  • Added gain error and offset error specifications.
		  • Removed signal to noise and distortion ratio (SNR) specifications.
		  • Removed Bipolar input mode specifications.
		• Updated "slow clock" to "core clock" in DPA Lock Time Specifications with DPA PLL Calibration Enabled diagram.
		• Updated the maximum values of the following conditions for Transmitter True Differential I/O Standards - f_{HSDR} (data rate) parameter in High-Speed I/O Specifications for Arria 10 Devices table.
		  • SERDES factor J = 2, uses DDR registers
		  • SERDES factor J = 1, uses DDR registers
		• Added the following tables:
		  • Memory Standards Supported by the Hard Memory Controller for Arria 10 Devices
		  • Memory Standards Supported by the Soft Memory Controller for Arria 10 Devices
		• Updated minimum T_{OCTCAL} value from 1000 cycles to 2000 cycles in OCT Calibration Block Specifications for Arria 10 Devices table.

Date	Version	Changes

		• Updated the hmc_free_clk specifications for the following speed grades in HPS Clock Performance for Arria 10 Devices table:
		  • –1 speed grade: Updated from 667 MHz to 533 MHz.
		  • –2 speed grade: Updated from 544 MHz to 533 MHz.
		• Changed from T_{sclk} to T_{clk} and added the following specifications in the Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria 10 Devices table.
		  • T_{qspi_clk}
		  • T_{din_start}
		  • T_{din_end}
		• Updated SPI Master Timing Requirements for Arria 10 Devices table.
		  • Changed the symbol from T_{spi_clk} to T_{clk}.
		  • Added note to $T_{dssfrst}$, T_{dsslst}, and T_h.
		  • Updated note to T_{su}.
		  • Updated the description for T_{su} and T_h.
		• Updated the note to T_{ssfsu}, T_{ssfh}, T_{sslsu}, and T_{sslh} in the SPI Slave Timing Requirements for Arria 10 Devices table.
		• Updated the following timing diagrams:
		  • Quad SPI Flash Serial Output Timing Diagram
		  • SPI Master Output Timing Diagram
		  • SPI Slave Output Timing Diagram
		• Added the following timing diagrams:
		  • Quad SPI Flash Serial Input Timing Diagram
		  • SPI Master Input Timing Diagram
		  • SPI Slave Input Timing Diagram

Date	Version	Changes

		• Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria 10 Devices table.
		    ◦ Changed T_{clk} to $T_{sdmmc\_clk\_out}$ and `TMMC_CLK` to `TSDMMC_CLK_OUT`.
		    ◦ Updated T_d min from 5.5 ns to 8.5 ns and max from 12.5 ns to 11.5 ns.
		    ◦ Updated note to T_d.
		• Changed the title and symbols in the following timing diagrams:
		    ◦ Changed from "NAND Data Input Cycle Timing Diagram" to "NAND Data Output Cycle Timing Diagram". Changed from D_{IN} to D_{OUT}.
		    ◦ Changed from "NAND Data Output Cycle Timing Diagram" to "NAND Data Input Cycle Timing Diagram". Changed from D_{OUT} to D_{IN}.
		    ◦ Changed from "NAND Extended Data Output (EDO) Cycle Timing Diagram" to "NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle". Changed from D_{OUT} to D_{IN}.
		• Changed from "ARM Trace Timing Characteristics" to "Trace Timing Characteristics".
		• Updated the description in the GPIO Interface topic.
		• Updated FPP Timing Parameters When the DCLK-to-DATA[] Ratio is 1 for Arria 10 Devices table.
		    ◦ Updated the maximum value for t_{STATUS} and t_{CF2ST1} from 1,506 µs to 3,000 µs.
		    ◦ Updated f_{MAX} for FPP ×8/×16 from 125 MHz to 100 MHz.
		    ◦ Updated the minimum value for t_{CF2CK} from 1,506 µs to 3,010 µs.
		    ◦ Updated the minimum value for t_{ST2CK} from 2 µs to 10 µs.
		    ◦ Updated the maximum value for t_{CD2UM} from 437 µs to 830 µs.
		• Updated FPP Timing Parameters When the DCLK-to-DATA[] Ratio is >1 for Arria 10 Devices table.
		    ◦ Updated the maximum value for t_{STATUS} and t_{CF2ST1} from 1,506 µs to 3,000 µs.
		    ◦ Updated f_{MAX} for FPP ×8/×16 from 125 MHz to 100 MHz.
		    ◦ Updated the minimum value for t_{CF2CK} from 1,506 µs to 3,010 µs.
		    ◦ Updated the minimum value for t_{ST2CK} from 2 µs to 10 µs.
		    ◦ Updated the maximum value for t_{CD2UM} from 437 µs to 830 µs.
		• Updated maximum value for t_{CD2UM} from 437 µs to 830 µs in AS Timing Parameters for AS ×1 and AS ×4 Configurations in Arria 10 Devices table.

Date	Version	Changes

		• Updated PS Timing Parameters for Arria 10 Devices table.
		  • Updated the maximum value for t_{STATUS} and t_{CF2ST1} from 1,506 µs to 3,000 µs
		  • Updated the minimum value for t_{CF2CK} from 1,506 µs to 3,010 µs.
		  • Updated the minimum value for t_{ST2CK} from 2 µs to 10 µs.
		  • Updated the maximum value for t_{CD2UM} from 437 µs to 830 µs.
		• Added description about **.rbf** and **.rpd** files in the Configuration Files section. Changed the table title from "Uncompressed Uncompressed .rbf Sizes Sizes for Arria 10 Devices" to "Configuration Bit Stream Sizes for Arria 10 Devices".
		• Updated the note to Active Serial in Minimum Configuration Time Estimation for Arria 10 Devices table. Note: The minimum configuration time is calculated based on DCLK frequency of 100 MHz. Only external `CLKUSR` may guarantee the frequency accuracy of 100 MHz. If you use internal oscillator of 100 MHz, you may not get the actual frequency of 100 MHz. For the DCLK frequency using internal oscillator, refer to the DCLK Frequency Specification in the AS Configuration Scheme table.
		• Changed instances of *Quartus II* to *Quartus Prime*.
		• Changed voltages and conditions in the "Transceiver Power Supply Operating Conditions for Arria 10 GX/SX Devices" table.
		• Changed maximum data rate conditions in the "Transmitter and Receiver Data Rate Performance" table.
		• Changed conditions in the "Transmitter and Receiver Data Rate Performance" table in the *Transceiver Performance for Arria 10 GT Devices* section.
		• Changed conditions in the "Reference Clock Specifications" table.
		• Changed the clock networks in the "Transceiver Clock Network Maximum Data Rate Specifications" table.
		• Changed conditions in the "Receiver Specifications" table.
		• Changed conditions in the "Transmitter Specifications" table.
		• Changed the minimum frequeny in the "ATX PLL Performance," "Fractional PLL Performance," and "CMU PLL Performance" tables in the *Transceiver Performance for Arria 10 GX/SX Devices* section.
		• Changed the minimum frequeny in the "ATX PLL Performance," "Fractional PLL Performance," and "CMU PLL Performance" tables in the *Transceiver Performance for Arria 10 GT Devices* section.
		• Added a parameter to the "Reference Clock Specifications" table.
		• Added footnote to the "Transmitter Specifications" table.

Date	Version	Changes

June 2015	2015.06.12	• Changed the specifications for the backplane maximum data rate condition in the "Transmitter and Receiver Data Rate Performance" table for Arria 10 GX/SX devices.
		• Changed the specifications for transmitter `REFCLK` phase noise in the "Reference Clock Specifications" table.
		• Added note in the following tables:
		  • Absolute Maximum Ratings for Arria 10 Devices: V_{CCPGM}
		  • Maximum Allowed Overshoot During Transitions for Arria 10 Devices: LVDS I/O
		  • Recommended Operating Conditions for Arria 10 Devices: V_I
		• Added HPS Specifications.
		• Updated recommended EPCQ-L serial configuration devices in the Uncompressed .rbf Sizes table.

May 2015	2015.05.08	Made the following changes: • Changed the specifications for the V_{ICM} (AC coupled) parameter in the "Reference Clock Specifications" table. • Changed the maximum frequency in the "CMU PLL Performance" table in the *Transceiver Performance for GT Devices* section. • Added a footnote to the transceiver speed grade 5 column in the "Transmitter and Receiver Data Rate Performance" table.
May 2015	2015.05.04	• Updated the Maximum Allowed Overshoot During Transitions for Arria 10 Devices table. • Added a note to t_{ramp} in the Recommended Operating Conditions for Arria 10 Devices table. Note: t_{ramp} is the ramp time of each individual power supply, not the ramp time of all combined power supplies. • Changed the minimum, typical, and maximum values for the transmitter and receiver power supply in the "Transceiver Power Supply Operating Conditions for Arria 10 GT Devices" table. • Added –1 speed grade in the condition column for V_{CCL_HPS} at 0.95 V in HPS Power Supply Operating Conditions for Arria 10 SX Devices table.

Date	Version	Changes

		• Added –I1S, –I2S, and –E2S speed grades to the following tables:
		  • Clock Tree Performance for Arria 10 Devices
		  • DSP Block Performance Specifications for Arria 10 Devices
		  • Memory Block Performance Specifications for Arria 10 Devices
		  • High-Speed I/O Specifications for Arria 10 Devices
		  • Memory Output Clock Jitter Specifications for Arria 10 Devices
		• Updated f_{IN} minimum value from 27 MHz to 50 MHz for all speed grades in the Fractional PLL Specifications for Arria 10 Devices table.
		• Changed the description for f_{INPFD} to "Input clock frequency to the PFD" in the I/O PLL Specifications for Arria 10 Devices table.
		• Updated DSP Block Performance Specifications for Arria 10 Devices table for V_{CC} and V_{CCP} at 0.9 V typical value. Added DSP specifications for V_{CC} and V_{CCP} at 0.95 V typical value.
		• Updated I_{bias} minimum value from 8 µA to 10 µA and maximum value from 200 µA to 100 µA in the External Temperature Sensing Diode Specifications for Arria 10 Devices table.
		• Added DPA (soft CDR mode) specifications in High-Speed I/O Specifications for Arria 10 Devices table.
		• Added description in POR Specifications section: Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.
		• Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria 10 Devices chapter.
		  • FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1
		  • FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1
		  • AS Configuration Timing Waveform
		  • PS Configuration Timing Waveform
		• Removed the DCLK-to-DATA[] ratio when both encryption and compression are turned on. Added description to the table: You cannot turn on encryption and compression at the same time for Arria 10 devices.

Date	Version	Changes

		• Updated the AS Timing Parameters for AS ×1 and AS ×4 Configurations in Arria 10 Devices table as follows:
		  • Changed the symbol for data hold time from t_H to t_{DH}.
		  • Updated the minimum value for t_{SU} from 0 ns to 1 ns.
		  • Updated the minimum value for t_{DH} from 2.5 ns to 1.5 ns.
		• Added a note to the DCLK Frequency Specification in the AS Configuration Scheme table. Note: You can only set 12.5, 25, 50, and 100 MHz in the Quartus Prime software.
		• Added a note to the Initialization Clock Source Option and the Maximum Frequency for Arria 10 Devices. Note: If you use the CLKUSR pin for AS and transceiver calibration simultaneously, the only allowed frequency is 100 MHz.
		• Changed Arria 10 GS to Arria 10 SX in Uncompressed .rbf Sizes and Minimum Configuration Time Estimation tables.
		• Added IO_IN_DLY_CHN and IO_OUT_DLY_CHN in the IOE Programmable Delay table.
		• Changed the Min/Typ/Max description for the V_{ICM} (AC coupled) parameter in the "Reference Clock Specifications" table.
		• Changed the Min/Typ/Max values in the "Transceiver Power Supply Operating Conditions for Arria 10 GX/SX Devices" table.
		• Changed the Min/Typ/Max values in the "Transceiver Power Supply Operating Conditions for Arria 10 GT Devices" table.
		• Added a footnote to the maximum data rate for GT channels in the "Transceiver Performance for GT Devices" section.
		• Made the following changes to the "Transceiver Performance for Arria 10 GX/SX Devices" section.
		  • Changed the maximum data rate condition for chip-to-chip and backplane in the "Transmitter and Receiver Data Rate Performance" table.
		  • Added TX minimum data rate to the "Transmitter and Receiver Data Rate Performance" table.
		  • Changed the minimum frequency in the "ATX PLL Performance" table.
		  • Changed the minimum frequency in the "Fractional PLL Performance" table.
		  • Changed the minimum and maximum frequency in the "CMU PLL Performance" table.

<table>
<tr><th>Date</th><th>Version</th><th>Changes</th></tr>
<tr><td></td><td></td><td>

Made the following changes to the "Transceiver Performance for Arria 10 GT Devices" section.

Added TX minimum data rate to the "Transmitter and Receiver Data Rate Performance" table.
Changed the maximum data rate condition for chip-to-chip and backplane in the "Transmitter and Receiver Data Rate Performance" table.
Changed the minimum frequency in the "ATX PLL Performance" table.
Changed the minimum frequency in the "Fractional PLL Performance" table.
Changed the minimum frequency in the "CMU PLL Performance" table.

Added voltage condition to the maximum peak-to-peak diff p-p after configuration and to the V_{ICM} specifications in the "Receiver Specifications" table.
Changed the voltage conditions for V_{OCM} in the "Transmitter Specifications" table.
Changed the V_{OD}/V_{CCT} Ratios in the "Typical Transmitter V_{OD} Settings" table.
Added the "Transceiver Clock Network Maximum Data Rate Specifications" table.

</td></tr>
<tr><td>January 2015</td><td>2015.01.23</td><td>

Added a note in the "Transceiver Power Supply Operating Conditions" section.
Made the following changes to the "Reference Clock Specifications" table:

Added the input reference clock frequency parameters for the CMU PLL, ATX PLL, and fPLL PLL.
Changed the maximum specification for rise time and fall time.
Added the V_{ICM} (AC and DC coupled) parameters.
Changed the maximum value for Transmitter REFCLK Phase Noise (622 MHz) when ≥ 1 MHz.

Changed the Min, Typ, and Max values for the <code>reconfig_clk</code> signal in the "Transceiver Clocks Specifications" table.
Made the following changes to the "Receiver Specifications" table:

Added the maximum peak-to-peak differential input voltage after device configuration specifications.
Changed the minimum specification for the minimum differential eye opening at receiver serial input pins parameter.
Removed the 120-ohm and 150-ohm conditions for the differential on-chip termination resistors parameter.
Added the V_{ICM} (AC and DC coupled) parameter.
Added the Programmable DC Gain parameter.

</td></tr>
</table>

Date	Version	Changes

		• Made the following changes to the "Transmitter Specifications" table:
		  • Added the V_{OCM} (AC coupled) parameter.
		  • Added the V_{OCM} (DC coupled) parameter.
		  • Changed the rise and fall time mimimum and maximum specifications.
		• Added the "Typical Transmitter V_{OD} Settings" table.
		• Added a note to V_{CC}, V_{CCP}, and V_{CCERAM} typical values in Recommended Operating Conditions table. Note: You can operate –1 and –2 speed grade devices at 0.9 V or 0.95 V typical value. You can operate -3 speed grade device at only 0.9 V typical value. Core performance shown in this datasheet is applicable for the operation at 0.9 V. Operating at 0.95 V results in higher core performance and higher power consumption. For more information about the performance and power consumption of 0.95 V operation, refer to the Quartus Prime software timing reports and Early Power Estimator (EPE).
		• Removed military grade operating junction temperature specifications (T_J) in Recommended Operating Conditions table.
		• Updated the V_{CCIO} range for HSTL-18 I/O standard in Differential HSTL and HSUL I/O Standards for Arria 10 Devices table as follows:
		  • Min: Updated from 1.425 V to 1.71 V
		  • Typ: Updated from 1.5 V to 1.8 V
		  • Max: Updated from 1.575 V to 1.89 V
		• Added a statement to Differential I/O Standards Specifications for Arria 10 Devices table: Differential inputs are powered by V_{CCPT} which requires 1.8 V.
		• Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.
		• Updated fractional PLL specifications.
		  • Updated f_{OUT_C} to f_{OUT} and updated the maximum value to 644 MHz for all speed grades.
		  • Updated f_{VCO} minimum value from 2.4 GHz to 3.125 GHz.
		  • Removed f_{OUT_L}, k_{VALUE}, and f_{RES} parameters.

Date	Version	Changes

		• Updated I/O PLL specifications.
		  • Updated f_{OUT_C} to f_{OUT} and updated the maximum value to 644 MHz for all speed grades.
		  • Updated f_{OUT_EXT} maximum value to 800 MHz (–1 speed grade), 720 MHz (–2 speed grade), and 650 MHz (–3 speed grade).
		  • Removed f_{RES} parameter.
		• Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design.
		• Updated AS Timing Parameters for AS x1 and AS x4 Configurations in Arria 10 Devices.
		  • Updated t_{SU} minimum value from 1.5 ns to 0 ns.
		  • Updated t_H minimum value from 0 ns to 2.5 ns.
		• Updated `CLKUSR` initialization clock source maximum frequency from 125 MHz to 100 MHz for passive configuration schemes (PS and FPP).
		• Added uncompressed **.rbf** sizes and minimum configuration time estimation for Arria 10 GX and GS devices.
		• Updated uncompressed **.rbf** sizes for Arria 10 GX 900 and 1150 devices, and Arria 10 GT 900 and 1150 devices.
		  • Updated configuration **.rbf** size from 335,106,890 bits to 351,292,512 bits.
		  • Updated IOCSR **.rbf** size from 6,702,138 bits to 1,885,396 bits.
		• Updated minimum configuration time estimation for Arria 10 GX 900 and 1150 devices, and Arria 10 GT 900 and 1150 devices for the following configuration modes:
		  • Active serial: Updated from 837.77 ms to 883.20 ms.
		  • Fast Passive Parallel: Updated from 104.72 ms to 110.40 ms.

Date	Version	Changes

August 2014	2014.08.18	• Changed the 3 V I/O conditions in Table 2.
		• Table 3:
		  • Added a note to the Minimum and Maximum operating conditions.
		  • Changed V_{CCERAM} values.
		  • Changed the Maximum recommended operating conditions for 3 V I/O V_I.
		• Added a note to the I/O pin pull-up tolerance in Table 12.
		• Changed the V_{IH} values for LVTTL, LVCMOS and 2.5 I/O standards in Table 13.
		• Table 14, Table 15, and Table 16:
		  • Added SSTL-12 I/O standard.
		  • Removed Class I, II for SSTL-135 and SSTL-125 I/O standards.
		• Table 19:
		  • Changed the minimum data rate specification for transmitter and receiver data rates.
		  • Changed the minimum frequency specification for the fractional PLL.
		  • Changed the minimum frequency specification for the CMU PLL.
		• Changed the Core Speed Grade with Power Options section in Table 20.
		• Table 21:
		  • Changed the minimum data rate specification for transmitter and receiver data rates.
		  • Changed the minimum frequency specification for the Fractional PLL.
		  • Changed the minimum frequency specification for the CMU PLL.
		  • Changed the minimum frequency of the ATX PLL.
		• Table 23:
		  • Added a note to the High Speed Differential I/O standard.
		  • Changed the specifications for CLKUSR pin.
		• Added columns in Table 29.
		• Changed the maximum f_{HSCLK_in} and $t_{xJitter}$ in Table 32.
		• Changed the minimum formula for t_{CD2UMC} in Table 42, Table 43, Table 44, and Table 46.
		• Changed the CLKUSR maximum frequency and minimum number of cycles in Table 47.

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		• Table 48:
		  • Changed the IOCSR **.rbf** size.
		  • Added Recommended EPCQ-L Serial Configuration Device.
		• Changed the DCLK frequency and minimum configuration time for FPP in Table 49.
		• Added the following tables:
		  • External Temperature Sensing Diode Specifications for Arria 10 Devices
		  • IOE Programmable Delay for Arria 10 Devices
		• Removed the following figures:
		  • CTLE Response in High Gain Mode for Arria 10 Devices with Data Rates ≥ 8 Gbps
		  • Removed the CTLE Response in High Gain Mode for Arria 10 Devices with Data Rates < 8 Gbps

March 2014	2014.03.14	Updated Table 3, Table 5, Table 21, Table 23, Table 24, Table 32, and Table 41.
December 2013	2013.12.06	Updated Figure 1 and Figure 2.
December 2013	2013.12.02	Initial release.