

### Preliminary Product Specifications

#### Features

- Ultra high-performance EPLD
  - 5 ns pin-to-pin speed on all fast inputs
  - 167 MHz maximum clock frequency
- 100% routable with 100% utilization
  - Eliminates pin-out changes during design iterations
- Incorporates four PAL-like 24V9 Fast Function Blocks
- 18 Output Macrocells
  - Programmable I/O architecture
  - 24 mA drive
- High-performance  $\mu$ P compatible
- Peripheral Component Interface (PCI) compatible
- JEDEC standard 3.3 V or 5 V I/O operation
- Multiple security bits for design protection
- 44-pin leaded chip carrier and 44-pin quad flat pack packages

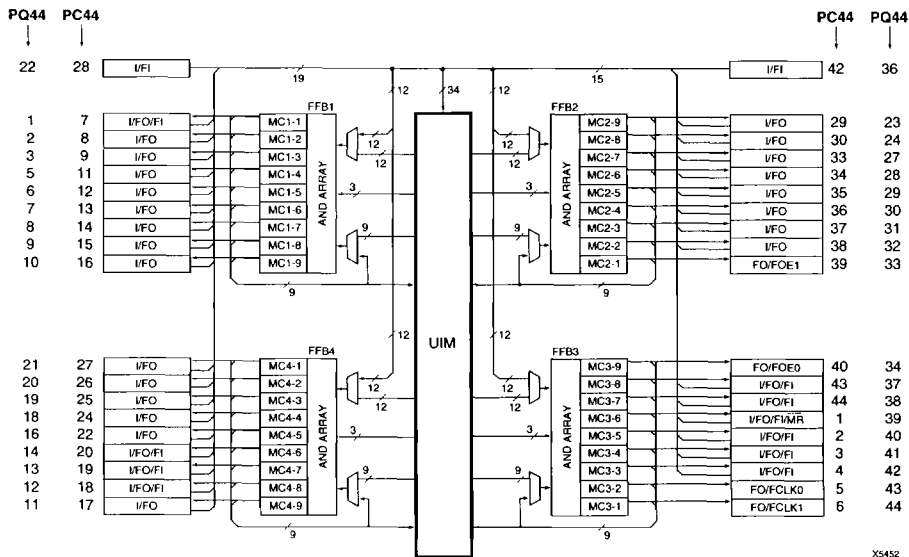
#### General Description

The XC7336 is a member of the Xilinx XC7300 EPLD family. It consists of four PAL-like 24V9 Fast Function Blocks interconnected by the 100%-populated Universal Interconnect Matrix (UIM™).

Each Fast Function Block has 24 inputs and contains nine Macrocells configurable for registered or combinational logic. The nine Macrocell outputs feed back to the UIM and can simultaneously drive the output pads.

The UIM allows 100% connectivity between all function blocks and input pins, providing the ability to utilize 100% of the device while eliminating routing issues.

Device logic is automatically configured to the user's specifications using the XEPLD software. The XEPLD V5.0 software is capable of optimizing and collapsing logic. The SMARTswitch software/hardware feature allows implementation of buried combinatorial logic functions in the UIM, thus increasing device utilization. The XEPLD software supports third party schematic capture and HDL entry tools, as well as direct equation-based text files. Using a workstation or PC platform, designs are automatically mapped into the XC7336 in a matter of minutes.



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Figure 1. XC7336 Functional Block Diagram

**Fast Function Blocks (FFB)**

The XC7336 provides four Fast Function Blocks which have 24 inputs that can be individually selected from the UIM, 12 fast input pins, or the 9 Macrocell feedbacks from the Function Block. The programmable AND array in each Fast Function Block generates 45 product terms to drive nine Macrocells in each FFB. Each Macrocell (Figure 2), can be configured for registered or combinatorial logic.

Five product terms from the programmable AND array are allocated to each Macrocell. Four of these product terms are ORed together and may be optionally inverted before driving the input of a programmable D-type flip-flop. The fifth product term drives the asynchronous active-High programmable Reset or Set Input to the Macrocell flip-flop. The flip-flop can be configured as a D-type or Toggle flip-flop or transparent for combinatorial outputs.

The programmable clock source is one of two global FastCLK signals (FCLK0 or FCLK1) that are distributed with short delay and minimal skew over the entire chip.

**I/O Block**

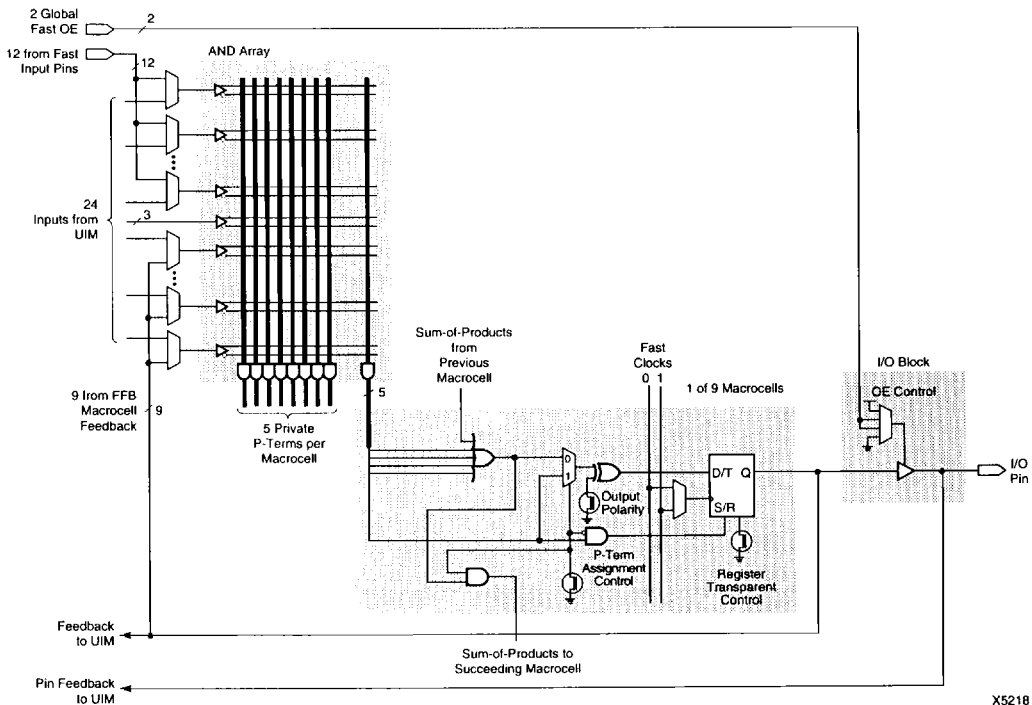
The Fast Function Block Macrocells drive chip outputs directly through 3-state output buffers. Each output buffer can be individually controlled by one of two dedicated active-High Fast Output Enable inputs or permanently

enabled or disabled. The Macrocell output can also be routed back as an input to the Fast Function Block, and the UIM.

**Power-On Characteristics/Master Reset**

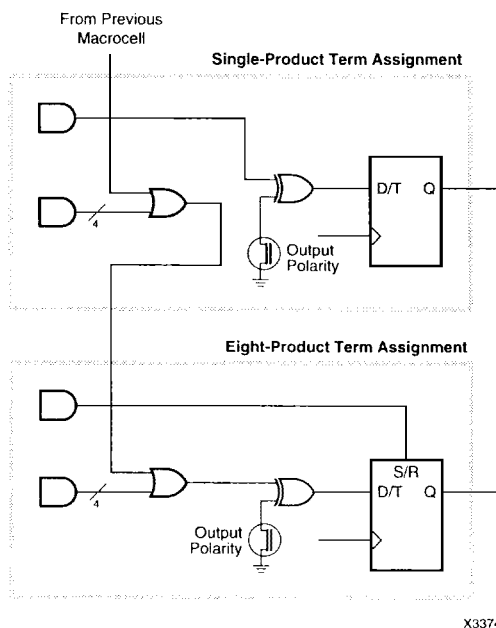
The XC7336 device undergoes a short internal initialization sequence upon device powerup. During this time ( $t_{RESET}$ ), the outputs remain 3-stated while the device is configured from its internal EPROM array and all registers are initialized. If the  $\overline{MR}$  pin is tied to  $V_{CCINT}$ , the initialization sequence is completely transparent to the user and is completed in  $t_{RESET}$  after  $V_{CCINT}$  has reached 4.75 V. If  $\overline{MR}$  is held low while the device is powering up, the internal initialization sequence begins and outputs will remain 3-stated until the sequence is complete and  $\overline{MR}$  is brought High.  $V_{CC}$  rise must be monotonic to insure the initialization sequence is performed correctly.

For additional flexibility, the  $\overline{MR}$  pin is provided so the EPLD can be reinitialized after power is applied. On the falling edge of  $\overline{MR}$ , all outputs become 3-stated and the initialization sequence is started. The outputs will remain 3-stated until the internal initialization sequence is complete and  $\overline{MR}$  is brought High. The minimum  $\overline{MR}$  pulse width is  $t_{WMR}$ . If  $\overline{MR}$  is brought High after  $t_{WMR}$ , but before  $t_{RESET}$ , the outputs will become active after  $t_{RESET}$ .



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Figure 2. Fast Function Block and Macrocell Schematic



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**Figure 3. Fast Function Block Product Term Assignment**

### Product Term Assignment

Each Macrocell sum-of-product OR gate can be expanded using the Export product-term assignment feature. The Export function transfers product-terms in increments of four from one Macrocell to the neighboring Macrocell (Figure 3). Complex logic functions requiring up to 36 product-terms can be implemented using all nine Macrocells within the Fast Function Block. When product-terms are assigned to adjacent Macrocells, the product-term normally dedicated to the Set or Reset function becomes the input to the Macrocell register.

### Universal Interconnect Matrix

The UIM receives input from Macrocell outputs, I/O pins, and dedicated input pins. Acting as an unrestricted crossbar switch, the UIM generates 24 output signals to each Fast Function Block. Each UIM input can be programmed to connect to any UIM output. The delay through the interconnect matrix is constant.

When multiple inputs are programmed to be connected to the same output, this output produces the logical AND of the input signals. By choosing the appropriate signal polarities at the input pins, Macrocell outputs and Fast Function Block AND-array inputs, this AND logic can also be used to implement wide NAND, OR or NOR functions. This offers an additional level of logic without additional speed penalty.

### 3.3 V or 5 V Interface Configuration

The XC7336 can be used in systems with two different supply voltages: 3.3 V and 5 V. Each XC7336 device has separate  $V_{CC}$  connections to the internal logic ( $V_{CCINT}$ ) and to the I/O pads ( $V_{CCIO}$ ).  $V_{CCINT}$  must always be connected to a 5 V supply.  $V_{CCIO}$  may be connected to either 3.3 V or 5 V, depending on the output interface requirement.

When  $V_{CCIO}$  is connected to 5 V, the input thresholds are TTL levels, and thus compatible with 3.3 V and 5 V logic. The output High levels are also TTL compatible. When  $V_{CCIO}$  is connected to 3.3 V, the input thresholds are still TTL levels, and the outputs pull up to the 3.3 V. This makes the XC7336 ideal for interfacing directly to 3.3 V components. In addition, the output structure is designed so that the I/O can also safely interface to a mixed 3.3 V and 5 V bus simultaneously.

### Design Security

The XC7336 has a multibit security system that controls access to the configuration programmed into the device. This security scheme uses multiple EPROM bits at various locations within the EPROM array to offer a higher degree of design security than other EPROM and fuser-based devices.

### Prototyping and Programming

Xilinx offers the HW-120 programmer for use during prototyping as well as support from major third party programmer companies. For production volumes, Xilinx and their licensed distributors offer factory programming of the XC7336 devices.

For factory programming procedures, contact your local Xilinx representative.

### XEPLD Translator Software

The designer can create, implement, and verify digital logic circuits for EPLD devices using the Xilinx XEPLD V5.0 software. Designs can be represented as schematics consisting of XEPLD library components, as behavioral descriptions (Boolean, HDL etc.), or as a combination of both techniques. The XEPLD translator automatically optimizes, collapses, and implements the design as well as writing a programming file without user intervention. At the completion of the compilation process, the XEPLD translator writes detailed report files for design analysis and documentation.

Here are just a few of the XEPLD Development System features:

- **Automatic Optimization and Mapping**  
Designs are automatically minimized and mapped into the devices for optimal efficiency and high performance. Critical logic functions are automatically assigned to special resources such as high speed clocks and global output enable signals. This allows the user to concentrate on design functionality without concern for physical implementation.
- **Automatic use of UIM Resources – SMARTswitch**  
The Universal Interconnect Matrix (UIM) used in Xilinx EPLDs provides an additional level of logic at no additional delay. XEPLD 5.0 automatically uses the inherent logic capability of the UIM when possible to reduce Macrocell requirements and increase speed.
- **N-to-1 PAL Conversion Utility**  
XEPLD automatically combines 20- and 24-pin standard PAL files into one top-level design file, checks for errors, and compiles the design into one or more EPLDs. The N-to-1 PAL converter is ideal for one step logic consolidation and board space reduction.
- **Complete Design Control**  
Users have the option to override the automatic features of XEPLD and selectively control any or all device resources.
- **Multiple Platform Support**  
XEPLD runs on IBM Compatible PCs, Sun, HP700, and IBM RS6000 platforms.

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest data sheet before finalizing a design.

### Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$V_{CC}$	Supply voltage with respect to GND	-0.5 to 7.0	V
$V_{IN}$	DC Input voltage with respect to GND	-0.5 to $V_{CC} + 5.0$	V
$V_{TS}$	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 5.0$	V
$T_{STG}$	Storage temperature	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+250	°C

**Warning.** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

### Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
$V_{CCINT}/V_{CCIO}$	Supply voltage relative to GND @ 5 V Commercial $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$	4.75	5.25	V
	Supply voltage relative to GND @ 5 V Industrial $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	4.50	5.50	V
	Supply voltage relative to GND @ 5 V Military $T_A = -55^\circ\text{C}$ to $T_C = +125^\circ\text{C}$	4.50	5.50	V
$V_{CCIO}$	I/O supply voltage relative to GND @ 3.3 V	3.0	3.60	V
$V_{IL}$	Low-level input voltage	0	0.80	V
$V_{IH}$	High-level input voltage	2.00	$V_{CC} + 0.5$	V
$V_O$	Output voltage	0	$V_{CCIO}$	V
$T_{IN}$	Input signal transition time		50	ns

## DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	5 V TTL High-level output voltage	$I_{OH} = -4.0$ mA $V_{CC} = \text{Min}$	2.4		V
	3.3 V High-level output voltage	$I_{OH} = -3.2$ mA $V_{CC} = \text{Min}$	2.4		V
$V_{OL}$	5 V TTL Low-level output voltage	$I_{OL} = 24$ mA $V_{CC} = \text{Min}$		0.5	V
	3.3 V Low-level output voltage	$I_{OL} = 24$ mA $V_{CC} = \text{Min}$		0.4	V
$I_L$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CCIO}$		$\pm 10.0$	$\mu\text{A}$
$I_{OZ}$	Output high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CCIO}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	Input capacitance for Input and I/O pins	$V_{IN} = \text{GND}$ $f = 1.0$ MHz		6.0	pF
$C_{IN}$	Input capacitance for global control pins (FCLK0, FCLK21, FOE0, FOE1)	$V_{IN} = \text{GND}$ $f = 1.0$ MHz		8.0	pF
$C_{OUT}^1$	Output capacitance	$V_{IN} = \text{GND}$ $f = 1.0$ MHz		10.0	pF
$I_{CC}^2$	Supply current	$V_{IN} = V_{CC}$ or GND $V_{CCINT} = V_{CCIO} = 5\text{V}$ $f = 1.0$ MHz @ 25°C		126 Typ	mA

## Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
$t_{WMR}$	Master Reset input Low pulse width	100			ns
$t_{RESET}^3$	Configuration completion time		80	160	$\mu\text{s}$

- Notes:
1. Sample tested.
  2. Measured with device programmed as a 16-bit counter.
  3. The initial state of the registers is user selectable. The default initialization is a logical 1.

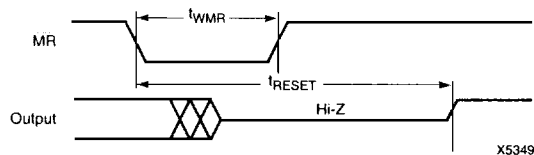


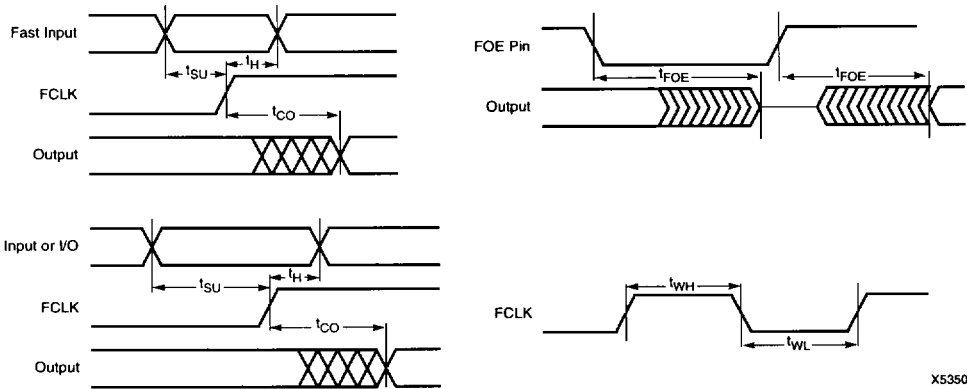
Figure 4. Global Reset Waveform

Fast Function Block (FFB) External AC Characteristics<sup>4</sup>

Symbol	Parameter	XC7336-5		XC7336-7		XC7336-10		XC7336-12		XC7336-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PD}$	Fast input to output valid <sup>5</sup>		5.0		7.5		10.0		12.0		15.0	ns
	I/O or input to output valid <sup>5</sup>		8.5		12.0		15.0		19.0		23.0	ns
$t_{SU}$	Fast input setup time before FCLK	3.5		4.0		5.0		6.0		7.0		ns
	I/O or input setup time before FCLK	7.0		8.5		10.0		13.0		15.0		ns
$t_H$	Fast, I/O or input hold time after FCLK	0		0		0		0		0		ns
$t_{CO}$	FCLK input to output valid		4.5		5.5		8.0		9.0		12.0	ns
$t_{FOE}$	Fast output enable/disable buffer delay		7.0		7.5		10.0		12.0		15.0	ns
$f_{MAX}$	Max count frequency <sup>5</sup>	167.0		125.0		100.0		80.0		66.7		ns
$t_{WLH}$	Fast Clock pulse width	3.0		4.0		5.0		5.5		6.0		ns

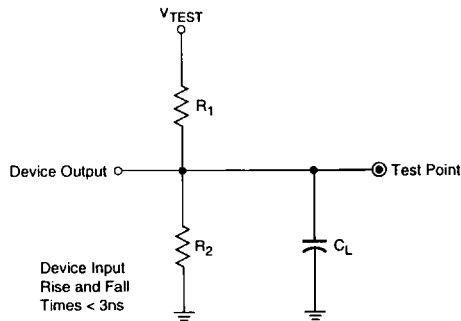
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- Notes: 4. All appropriate ac specifications tested using Figure 6 as test load circuit.  
 5. Assumes four product terms per output.



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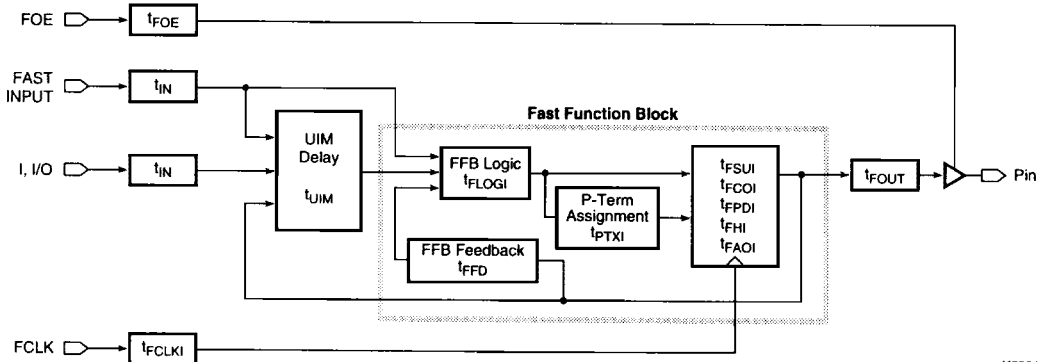
Figure 5. Switching Waveforms



V <sub>CCIO</sub> Level	V <sub>TEST</sub>	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub>
5 V	5.0 V	160 Ω	120 Ω	35 pF
3.3 V	3.3 V	260 Ω	360 Ω	35 pF

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Figure 6. AC Load Circuit



X5221

Figure 7. XC7336 Timing Model

### Timing Model

Timing within the XC7336 is accurately determined using external timing parameters from the device data sheet, using a variety of CAE simulators, or with the timing model shown in Figure 7.

The timing model is based on the fixed internal delays of the XC7336 architecture which consists of three basic parts: I/O Blocks, the UIM and Fast Function Blocks. The timing model identifies the internal delay paths and their relationships to ac characteristics. Using this model and the ac characteristics, designers can easily calculate the timing information for the XC7336.

### Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC7336-5		XC7336-7		XC7336-10		XC7336-12		XC7336-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{FLOGI}$	FFB logic array delay <sup>(6)</sup>		1.0		1.5		1.5		2.0		2.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay <sup>(6)</sup>		2.0		3.5		5.5		7.0		8.0	ns
$t_{FSUI}$	FFB register setup time	2.5		1.5		2.5		3.0		4.0		ns
$t_{FHI}$	FFB register hold time	1.0		2.5		2.5		3.0		3.0		ns
$t_{FCOI}$	FFB register clock-to-output delay		1.0		1.0		1.0		1.0		1.0	ns
$t_{FPDI}$	FFB register pass through delay		0.5		0.5		0.5		1.0		1.0	ns
$t_{FAOI}$	FFB register async. set delay		2.0		2.0		2.5		3.0		4.0	ns
$t_{PTXI}$	FFB p-term assignment delay		0.6		0.8		1.0		1.2		1.5	ns
$t_{FFD}$	FFB feedback delay		0.5		4.0		5.0		6.5		8.0	ns

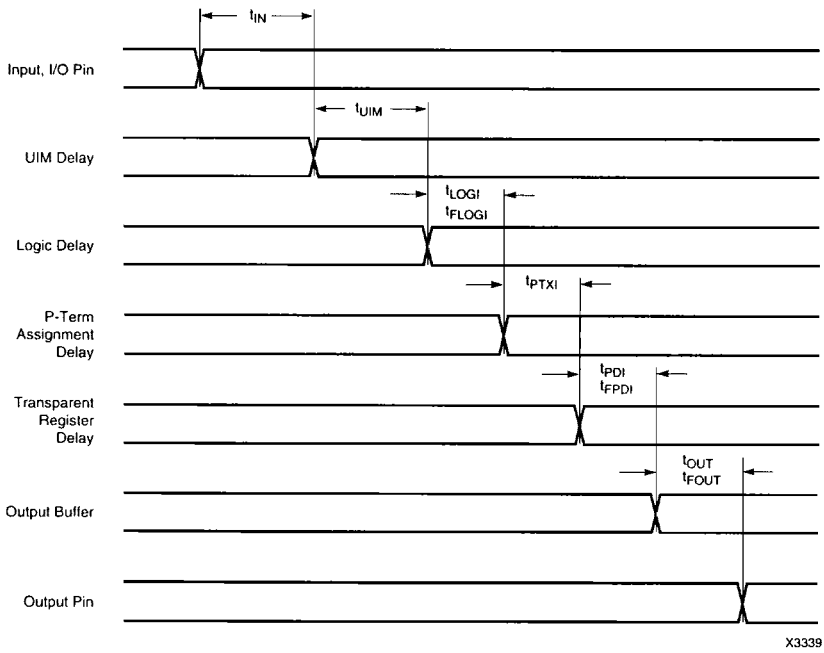
Notes: 6. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

### Internal AC Characteristics

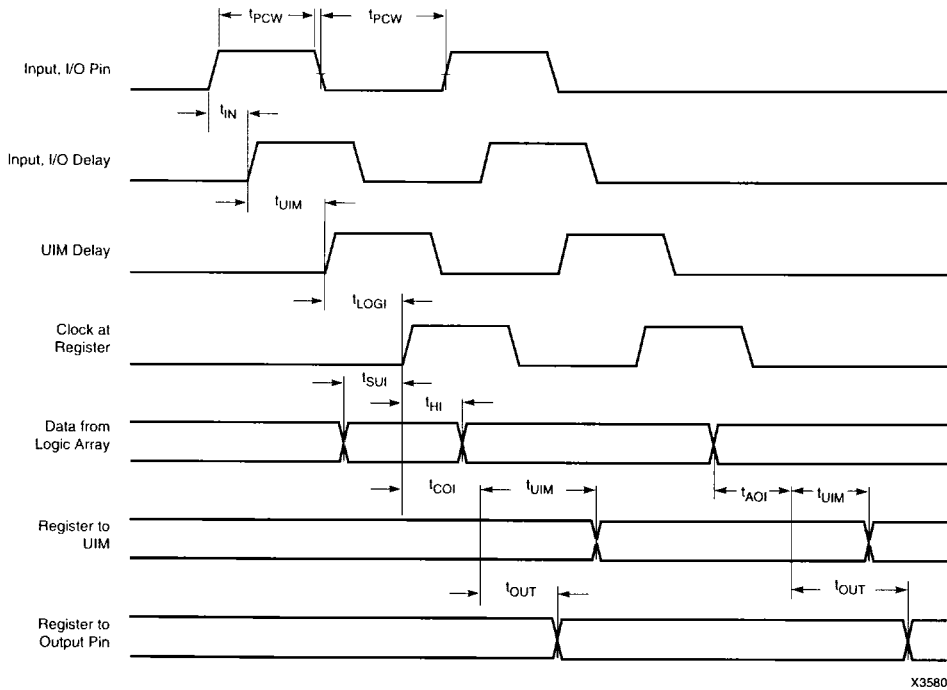
Symbol	Parameter	XC7336-5		XC7336-7		XC7336-10		XC7336-12		XC7336-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay		1.5		2.5		3.5		4.0		5.0	ns
$t_{FOUT}$	FFB output buffer and pad delay		2.0		3.0		4.5		5.0		7.0	ns
$t_{UIM}$	Universal Interconnect Matrix delay		3.5		4.5		5.0		7.0		8.0	ns
$t_{FCLKI}$	Fast clock buffer delay		1.5		1.5		2.5		3.0		4.0	ns

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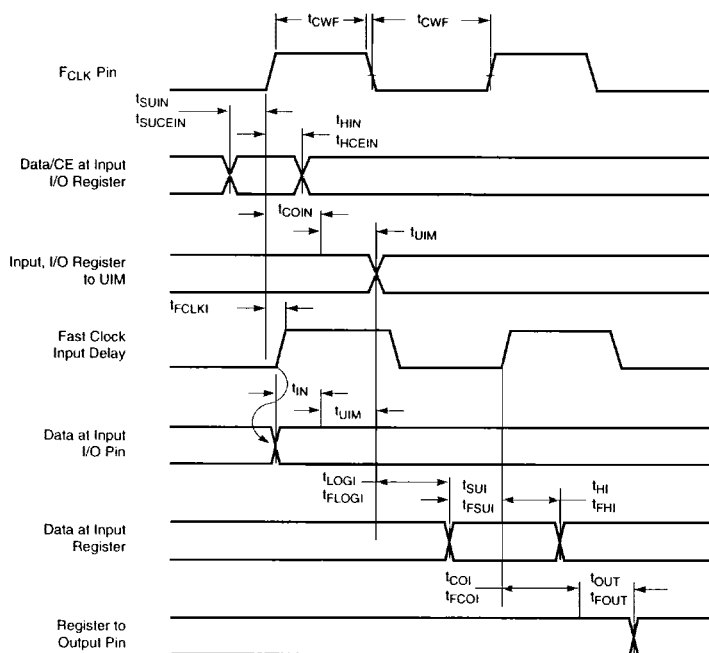
Combinatorial Switching Characteristics



Asynchronous Clock Switching Characteristics



## Synchronous Clock Switching Characteristics



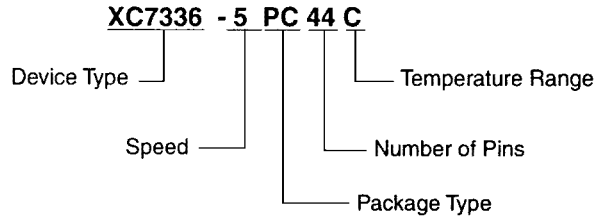
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## XC7336 Pinouts

PQ44	PC44	Input	XC7336	Output
39	1	I/FO/FI	MR	MC3-6
40	2	I/FO/FI		MC3-5
41	3	I/FO/FI		MC3-4
42	4	I/FO/FI		MC3-3
43	5	FO/FCLK0		MC3-2
44	6	FO/FCLK1		MC3-1
1	7	I/FO/FI		MC1-1
2	8	I/FO		MC1-2
3	9	I/FO		MC1-3
4	10		GND	
5	11	I/FO		MC1-4
6	12	I/FO		MC1-5
7	13	I/FO		MC1-6
8	14	I/FO		MC1-7
9	15	I/FO		MC1-8
10	16	I/FO		MC1-9
11	17	I/FO		MC4-9
12	18	I/FO/FI		MC4-8
13	19	I/FO/FI		MC4-7
14	20	I/FO/FI		MC4-6
15	21		V <sub>CCINT</sub>	
16	22	I/FO		MC4-5

PQ44	PC44	Input	XC7336	Output
17	23		GND	
18	24	I/FO		MC4-4
19	25	I/FO		MC4-3
20	26	I/FO		MC4-2
21	27	I/FO		MC4-1
22	28	I/FI		
23	29	I/FO		MC2-9
24	30	I/FO		MC2-8
25	31		GND	
26	32		V <sub>CCIO</sub>	
27	33	I/FO		MC2-7
28	34	I/FO		MC2-6
29	35	I/FO		MC2-5
30	36	I/FO		MC2-4
31	37	I/FO		MC2-3
32	38	I/FO		MC2-2
33	39	FO/FOE1		MC2-1
34	40	FO/FOE0		MC3-9
35	41		V <sub>CCINT</sub> /V <sub>PP</sub>	
36	42	I/FI		
37	43	I/FO/FI		MC3-8
38	44	I/FO/FI		MC3-7

**Ordering Information**



**Speed Options**

- 15 15 ns pin-to-pin delay
- 12 12 ns pin-to-pin delay
- 10 10 ns pin-to-pin delay (commercial and industrial only)
- 7 7.5 ns pin-to-pin delay (commercial only)
- 5 5 ns pin-to-pin delay (commercial only)

**Packaging Options**

- PC44 44-Pin Plastic Leaded Chip Carrier
- WC44 44-Pin Windowed Ceramic Leaded Chip Carrier
- PQ44 44-Pin Plastic Quad Flat Pack

**Temperature Options**

- C Commercial 0°C to 70°C
- I Industrial -40°C to 85°C
- M Military -55°C (Ambient) to +125°C (Case)

**Component Availability**

Pins	44			68		84		100	144	160	184	225	
	Plastic PLCC	Ceramic CLCC	Plastic PQFP	Plastic PLCC	Ceramic CLCC	Plastic CLCC	Ceramic PGA	Plastic PQFP	Ceramic PGA	Plastic PQFP	Ceramic PGA	Plastic BGA	Ceramic BGA
Code	PC44	WC44	PQ44	PC68	WC84	PC84	WC84	PQ100	PG144	PQ160	PG184	BG225	WB225
XC7336	-15	CI	CI(M)	C									
	-12	CI	CI(M)	C									
	-10	CI	CI(M)	C									
	-7	C	C	C									
	-5	C	C	C									

C = Commercial = 0° to +70°C I = Industrial = -40° to 85°C

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