XC1700E Family of Serial Configuration PROMs

December 7, 1998 (Version 1.4) | Product Specification

Features

- Serial Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams of Xilinx FPGA devices
- Simple interface to the FPGA requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- The XC17128E/EL and XC17256E/EL devices support the XC4000EX/XL/XLA/XV fast configuration mode (15.0 MHz)
- Low-power CMOS floating gate process
- Available in 5 V and 3.3 V versions
- Available in compact plastic 8-pin DIP, 8-pin SOIC, 8-pin VOIC, or 20-pin PLCC packages.
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.

Description

The XC1700 family of serial configuration PROMs (SPROMs) provides an easy-to-use, cost-effective method for storing Xilinx FPGA configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the SPROM. A short access time after the rising clock edge, data appears on the SPROM DATA output pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the SPROM. When the FPGA is in Slave Serial mode, the SPROM and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all SPROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx Alliance or the Foundation series development systems compiles the FPGA design file into a standard HEX format which is then transferred to most commercial PROM programmers.

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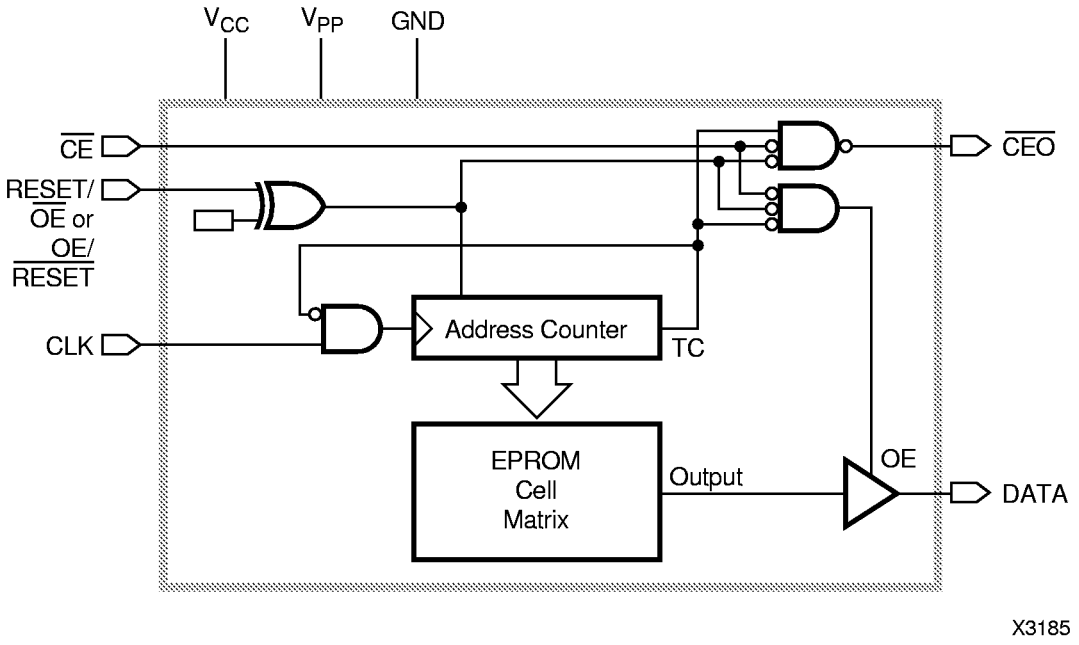


Figure 1: Simplified Block Diagram (does not show programming circuit)

Pin Description

DATA

Data output, 3-stated when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

CLK

Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.

RESET/$\overline{OE}$

When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is 3-stated. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be driven by the FPGA's $\overline{INIT}$ pin.

The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 programmer software. Third-party programmers have different methods to invert this pin.

$\overline{CE}$

When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low-I_{CC} standby mode.

$\overline{CEO}$

Chip Enable output, to be connected to the $\overline{CE}$ input of the next SPROM in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When $\overline{OE}$ goes inactive, $\overline{CEO}$ stays High until the PROM is reset. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

V_{PP}

Programming voltage. No overshoot above the specified max voltage is permitted on this pin. For normal read operation, this pin *must* be connected to V_{CC}. Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. *Do not leave VPP floating!*

V_{CC} and GND

V_{CC} is positive supply pin and GND is ground pin.

Serial PROM Pinouts

Pin Name	8-Pin	20-Pin
DATA	1	2
CLK	2	4
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	3	6
$\overline{CE}$	4	8
GND	5	10
$\overline{CEO}$	6	14
V_{PP}	7	17
V_{CC}	8	20

Capacity

Device	Configuration Bits
XC1736E	36,288
XC1765E or EL	65,536
XC17128E or EL	131,072
XC17256E or EL	262,144
XC17512L	524,288
XC1701, XC1701L or XQ1701L	1,048,576
XC1702L	2,097,152
XC1704L	4,194,304

Note: The XC17512L and larger SPROMs are specified in a separate datasheet.

Number of Configuration Bits, Including Header for Xilinx FPGAs and Compatible SPROMs

Device	Configuration Bits	SPROM
XC4003E	53,984	XC17128E[1]
XC4005E	95,008	XC17128E
XC4006E	119,840	XC17128E
XC4008E	147,552	XC17256E
XC4010E	178,144	XC17256E
XC4013E	247,968	XC17256E
XC4020E	329,312	XC1701
XC4025E	422,176	XC1701
XC4002XL	61,100	XC17128EL[1]
XC4005XL	151,960	XC17256EL
XC4010XL	283,424	XC17512L
XC4013XL/XLA	393,632	XC17512L
XC4020XL/XLA	521,880	XC17512L
XC4028XL/XLA	668,184	XC1701L
XC4028EX	668,184	XC1701
XC4036EX/XL/XLA	832,528	XC1701L
XC4036EX	832,528	XC1701
XC4044XL/XLA	1,014,928	XC1701L
XC4052XL/XLA	1,215,368	XC1702L
XC4062XL/XLA	1,433,864	XC1702L
XC4085XL/XLA	1,924,992	XC1702L
XC40110XV	2,686,136	XC1704L
XC40150XV	3,373,448	XC1704L
XC40200XV	4,551,056	XC1704L + XC17512L
XC40250XV	5,433,888	XC1704L+ XC1702L
XC5202	42,416	XC1765E
XC5204	70,704	XC17128E
XC5206	106,288	XC17128E
XC5210	165,488	XC17256E
XC5215	237,744	XC17256E
XCV50	559,232	XC1701L
XCV100	781,248	XC1701L
XCV150	1,041,128	XC1701L
XCV200	1,335,872	XC1702L
XCV300	1,751,840	XC1702L
XCV400	2,546,080	XC1704L
XCV600	3,608,000	XC1704L
XCV800	4,715,648	XC1704L + XC1701L
XCV1000	6,127,776	XC1704L + XC1702L

Note: 1. The suggested SPROM is determined by compatibility with the higher configuration frequency of the Xilinx FPGA CCLK. Designers using the default slow configuration frequency (CCLK) can use the XC1765E or XC1765EL for the noted FPGA devices.
2. The XC1701, XC1701L, XC1702L, XC1704L & XC17512L are specified in a separate XC1700L High Density datasheet.

Controlling Serial PROMs

Connecting the FPGA device with the SPROM.

- The DATA output(s) of the SPROM(s) drives the DIN input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the SPROM(s).
- The $\overline{CEO}$ output of a SPROM drives the $\overline{CE}$ input of the next SPROM in a daisy chain (if any).
- The $\overline{RESET}$/OE input of all SPROMs is best driven by the $\overline{INIT}$ output of the lead FPGA device. This connection assures that the SPROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch. Other methods – such as driving $\overline{RESET}$/OE from $\overline{LDC}$ or system reset – assume the SPROM internal power-on-reset is always in step with the FPGA's internal power-on-reset. This may not be a safe assumption.
- The SPROM $\overline{CE}$ input can be driven from either the $\overline{LDC}$ or DONE pins. Using $\overline{LDC}$ avoids potential contention on the DIN pin.
- The $\overline{CE}$ input of the lead (or only) SPROM is driven by the DONE output of the lead FPGA device, provided that DONE is not permanently grounded. Otherwise, $\overline{LDC}$ can be used to drive $\overline{CE}$, but must then be unconditionally High during user operation. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. The Xilinx SPROMs have been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the SPROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the SPROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. Xilinx FPGAs take care of this automatically with an on-chip default pull-up resistor.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple FPGA-configurations for a single FPGA are stored in a SPROM, the $\overline{OE}$ pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{OE}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies $\overline{RESET}$ during the FPGA configuration process. The FPGA aborts the configuration and then restarts a new configuration, as intended, but the SPROM does not reset its address counter, since it never saw a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the FPGA is the master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and DONE goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

Cascading Serial Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded SPROMs provide additional memory. After the last bit from the first SPROM is read, the next clock signal to the SPROM asserts its $\overline{CEO}$ output Low and disables its DATA line. The second SPROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded SPROMs are reset if the FPGA $\overline{RESET}$ pin goes Low, assuming the SPROM reset polarity option has been inverted.

To reprogram the FPGA with another program, the DONE line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DIN.

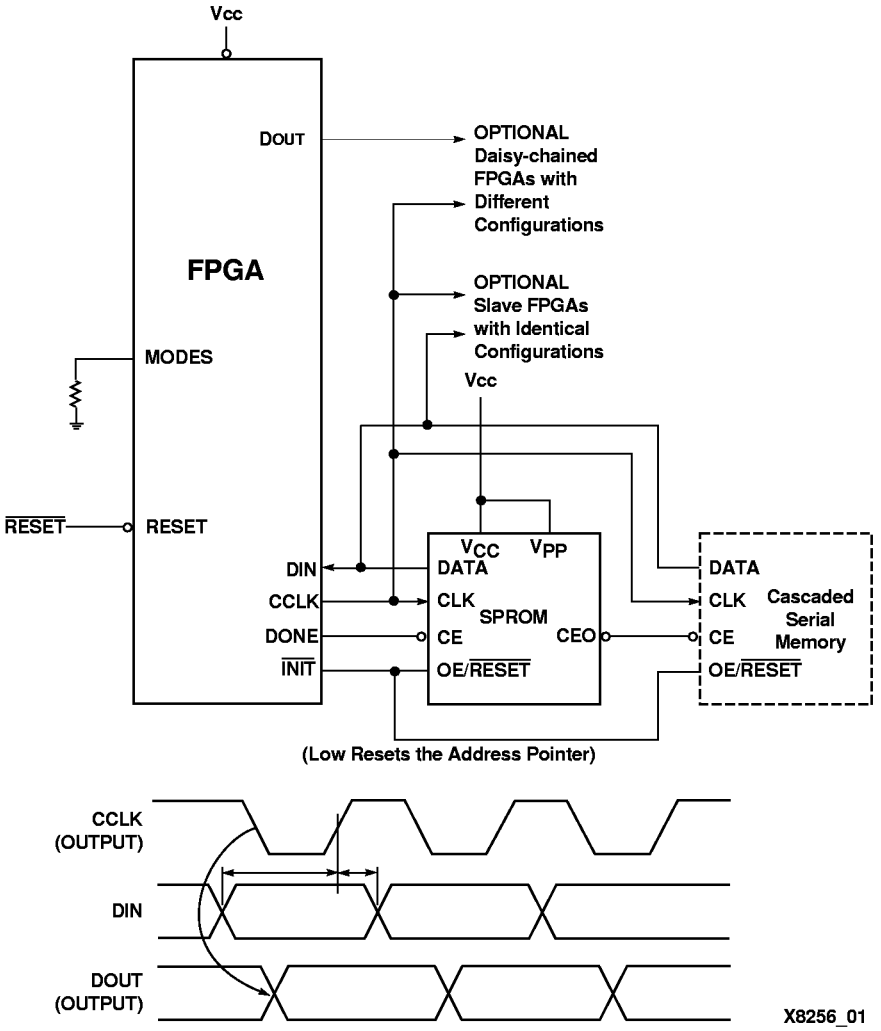


Figure 2: Master Serial Mode. The one-time-programmable SPROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional FPGAs. An early DONE inhibits the SPROM data output one CCLK cycle before the FPGA I/Os become active.

Standby Mode

The SPROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Programming

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

Table 1: Truth Table for XC1700 Control Inputs

Control Inputs		Internal Address	Outputs		
RESET	CE		DATA	CEO	I_{cc}
Inactive	Low	if address ≤ TC: increment if address > TC: don't change	active 3-state	High Low	active reduced
Active	Low	Held reset	3-state	High	active
Inactive	High	Not changing	3-state	High	standby
Active	High	Held reset	3-state	High	standby

Notes: 1. The XC1700 RESET input has programmable polarity
2. TC = Terminal Count = highest address value. TC+1 = address 0.

Important: Always tie the V_{PP} pin to V_{CC} in your application. Never leave V_{PP} floating.

XC1736E, XC1765E, XC17128E and XC17256E

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND	-0.5 to +12.5	V
V_{IN}	Input voltage relative to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND (T_A = 0°C to +70°C)	4.75	5.25	V
	Industrial	Supply voltage relative to GND (T_A = -40°C to +85°C)	4.50	5.50	V

Note: During normal read operation V_{PP} ***must*** be connected to V_{CC}

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
I_{CCA}	Supply current, active mode (at maximum frequency)			10.0	mA
I_{CCS}	Supply current, standby mode			50.0	µA
I_L	Input or output leakage current		-10.0	10.0	µA
C_{IN}	Input Capacitance (V_{IN} = GND, f = 1.0MHz)			10.0	pF
C_{OUT}	Output Capacitance (V_{IN} = GND, f = 1.0MHz)			10.0	pF

XC1765EL, XC17128EL and XC17256EL

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +4.0	V
V_{PP}	Supply voltage relative to GND	-0.5 to +12.5	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

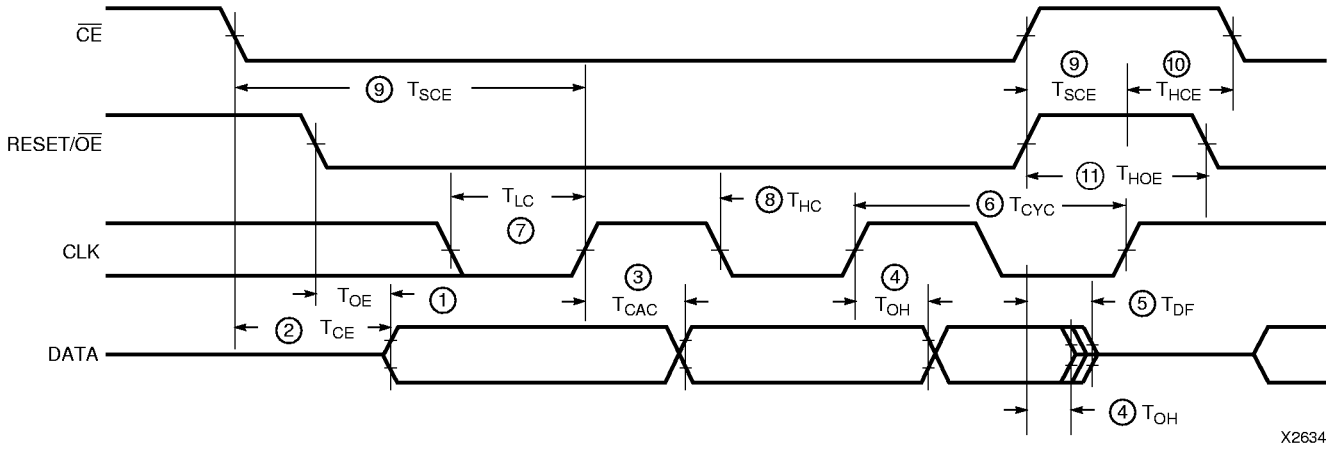
Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND (T_A = 0°C to +70°C)	3.0	3.6	V
	Industrial	Supply voltage relative to GND (T_A = -40°C to +85°C)	3.0	3.6	V

Note: During normal read operation V_{PP} ***must*** be connected to V_{CC}

DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
V_{IH}	High-level input voltage	2.0	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -3 mA)	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)		0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency)		5.0	mA
I_{CCS}	Supply current, standby mode		50.0	µA
I_L	Input or output leakage current	-10.0	10.0	µA
C_{IN}	Input Capacitance (V_{IN} = GND, f = 1.0MHz)		10.0	pF
C_{OUT}	Output Capacitance (V_{IN} = GND, f = 1.0MHz)		10.0	pF

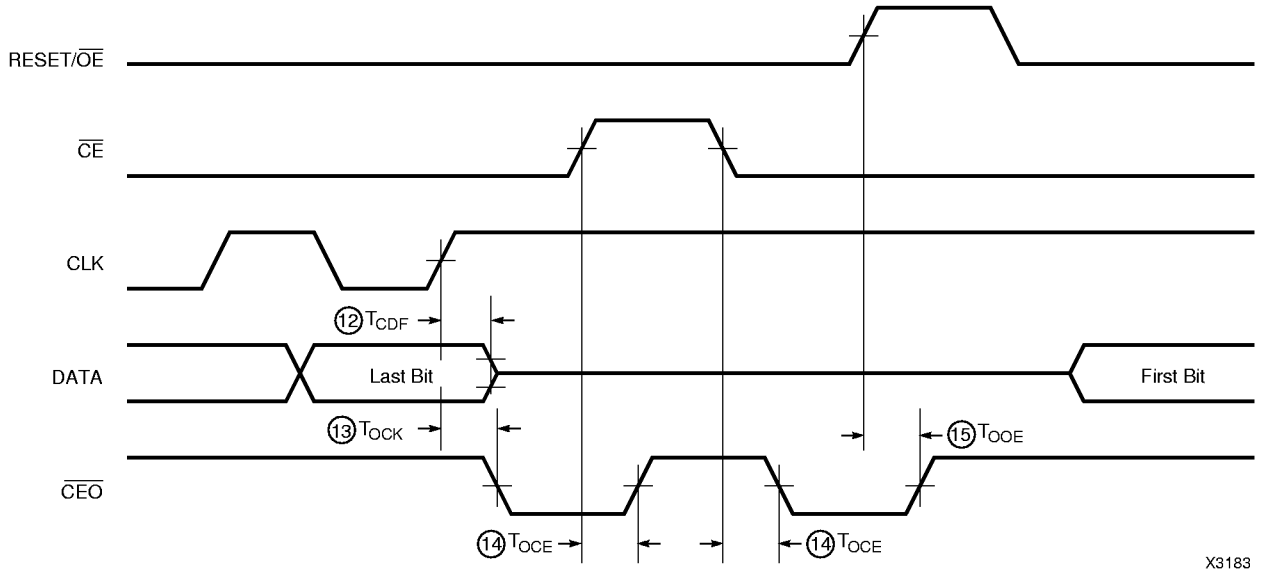
AC Characteristics Over Operating Condition



Symbol		Description	XC1736E XC1765E		XC1765EL		XC17128E XC17256E		XC17128EL XC17256EL		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
1	T_{OE}	$\overline{OE}$ to Data Delay		45		45		25		30	ns
2	T_{CE}	$\overline{CE}$ to Data Delay		60		60		45		45	ns
3	T_{CAC}	CLK to Data Delay		80		200		45		45	ns
4	T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK[3]	0		0		0		0		ns
5	T_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay[2 & 3]		50		50		50		50	ns
6	T_{CYC}	Clock Periods	100		400		67		67		ns
7	T_{LC}	CLK Low Time[3]	50		100		20		25		ns
8	THC	CLK High Time[3]	50		100		20		25		ns
9	TSCE	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25		40		20		25		ns
10	T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		0		0		0		ns
11	T_{HOE}	$\overline{OE}$ Hold Time (guarantees counters are reset)	100		100		20		25		ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at +/- 200mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.

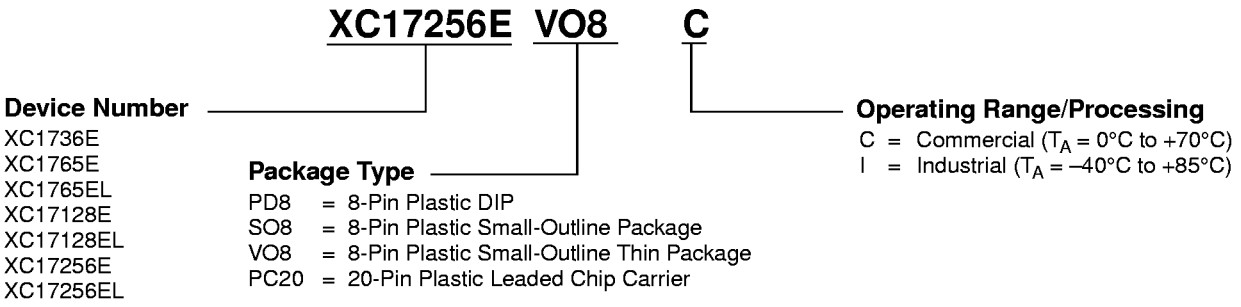
AC Characteristics Over Operating Condition When Cascading



Symbol		Description	Min	Max	Units
12	T_{CDF}	CLK to Data Float Delay[2, 3]		50	ns
13	T_{OCK}	CLK to $\overline{CEO}$ Delay[3]		30	ns
14	T_{OCE}	CE to $\overline{CEO}$ Delay[3]		35	ns
15	T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay[3]		30	ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at +/- 200mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.

Ordering Information



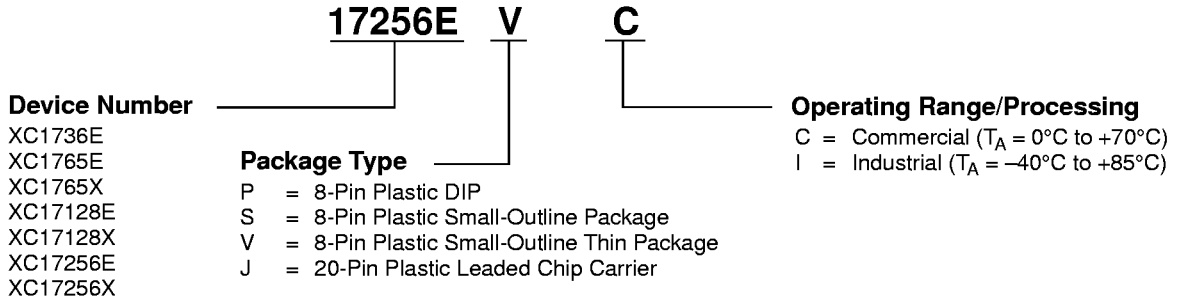
Valid Ordering Combinations

XC17128EPD8C	XC17256EPD8C	XC1736EPD8C	XC1765EPD8C	XC1701PD8C	XC1702LVQ44C
XC17128EVO8C	XC17256EVO8C	XC1736ESO8C	XC1765ESO8C	XC1701PC20C	XC1702LPC44C
XC17128EPC20C	XC17256EPC20C	XC1736EVO8C	XC1765EVO8C	XC1701SO20C	XC1704LVQ44C
XC17128EPD8I	XC17256EPD8I	XC1736EPC20C	XC1765EPC20C	XC1701PD8I	XC1704LPC44C
XC17128EVO8I	XC17256EVO8I	XC1736EPD8I	XC1765EPD8I	XC1701PC20I	XC1702LVQ44I
XC17128EPC20I	XC17256EPC20I	XC1736ESO8I	XC1765ESO8I	XC1701SO20I	XC1702LPC44I
		XC1736EVO8I	XC1765EVO8I		XC1704LVQ44I
		XC1736EPC20I	XC1765EPC20I		XC1704LPC44I
XC17128ELPD8C	XC17256ELPD8C		XC1765ELPD8C	XC1701LPD8C	XC17512LPD8C
XC17128ELVO8C	XC17256ELVO8C		XC1765ELSO8C	XC1701LPC20C	XC17512LPC20C
XC17128ELPC20C	XC17256ELPC20C		XC1765ELVO8C	XC1701LSO20C	XC17512LSO20C
XC17128ELPD8I	XC17256ELPD8I		XC1765ELPC20C	XC1701LPD8I	XC17512LPD8I
XC17128ELVO8I	XC17256ELVO8I		XC1765ELPD8I	XC1701LPC20I	XC17512LPC20I
XC17128ELPC20I	XC17256ELPC20I		XC1765ELSO8I	XC1701LSO20I	XC17512LSO20I
			XC1765ELVO8I	XQ1701LCC44M	
			XC1765ELPC20I	XQ1701LCC44B	
				XQ1701LS020N	

Note: The XC1701, XC1701L, XQ1701L, XC1702L, XC1704L and XC17512L products are specified in the XC1700L High Density datasheet.

Marking Information

Due to the small size of the serial PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.

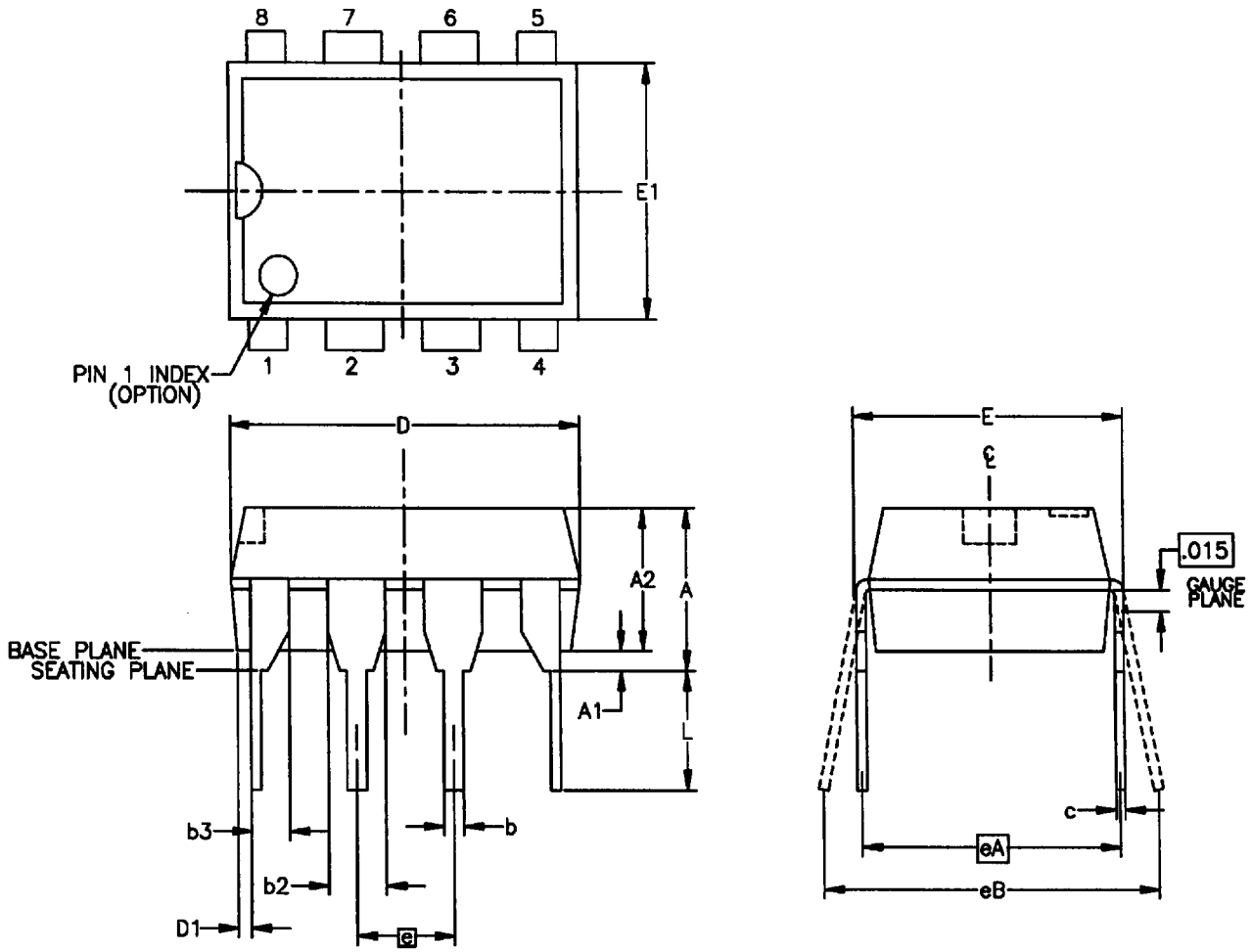


Note: When marking the device number on the EL parts, an X is used in place of an EL.

Revision Control

Date	Revision
7/14/98	Revised I_{CCS} on page 19 and page 20; revised V_{CC} specifications for T_A on page 19 and page 20; revised V_{CC} on page 19; revised Note 2 on page 20 and page 21; added T_A to operating range specifications on page 23.
9/8/98	Revised the references to FPGAs to include the XC4000XLA and XC4000XV families.
9/30/98	Updated the Valid Ordering Combinations onpage 23 to include high density products.
12/7/98	Updated the references to compatible FPGAs to include the Virtex family.

Plastic DIP Package - PD8



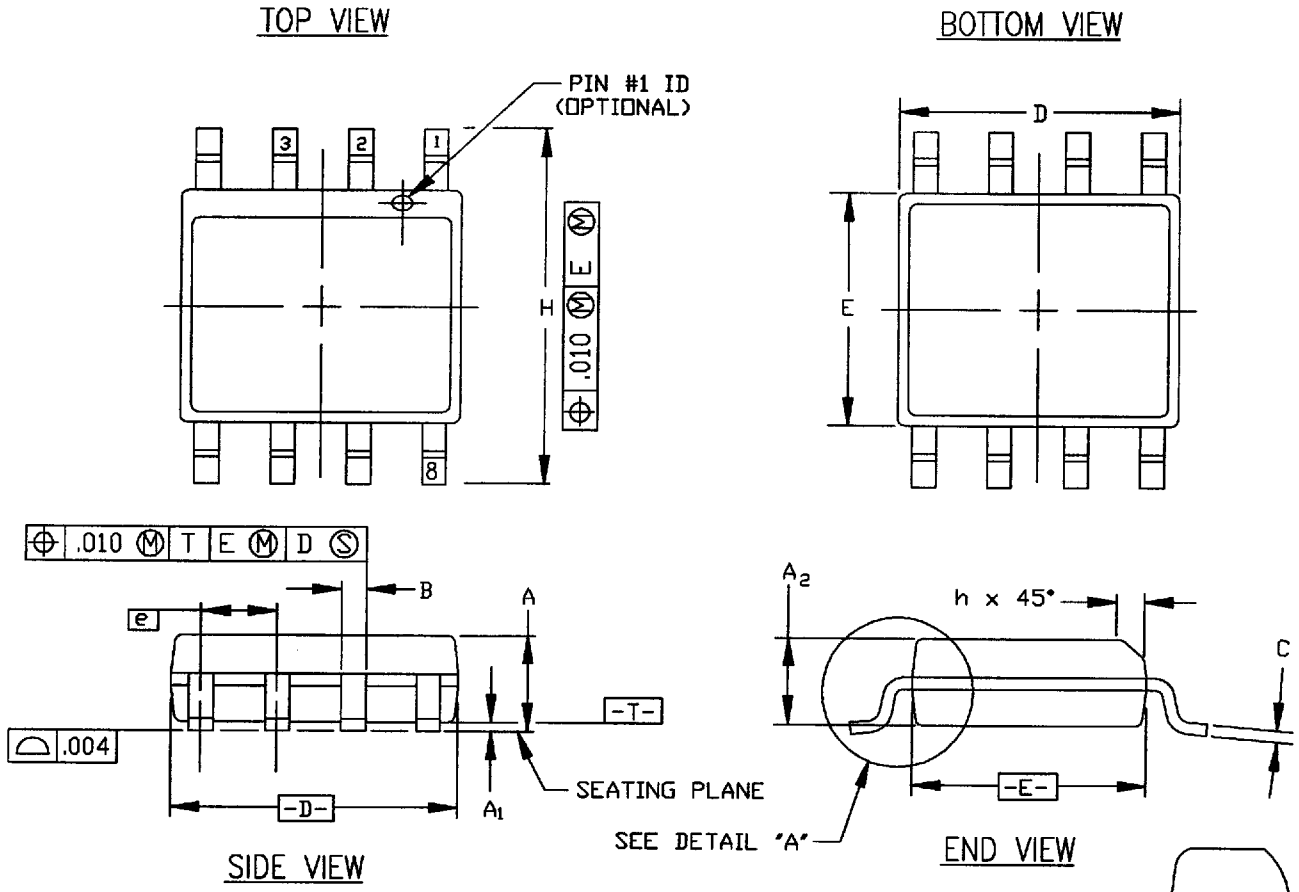
SYMBOL	INCHES		NOTE
	MIN.	MAX.	
A	—	0.181	
A_1	0.019	—	
A_2	0.122	0.161	
b	0.014	0.022	
b_2	0.045	—	
b_3	—	0.045	
c	0.009	0.012	
D	0.355	0.382	
D_1	0.005	—	
E	0.303	0.323	
E_1	0.240	0.272	
e	0.100 BSC		
e_A	0.300 BSC		
e_B	—	0.430	
L	0.115	0.150	
N	8		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED .010" PER SIDE.
3. LEAD FINISH: (85±5%)Sn-Pb SOLDER PLATE
4. CONFORMS TO JEDEC MS-001-BA

8-PIN PLASTIC DIP (PD8)

SOIC and TSOP Packages - SO8, VO8



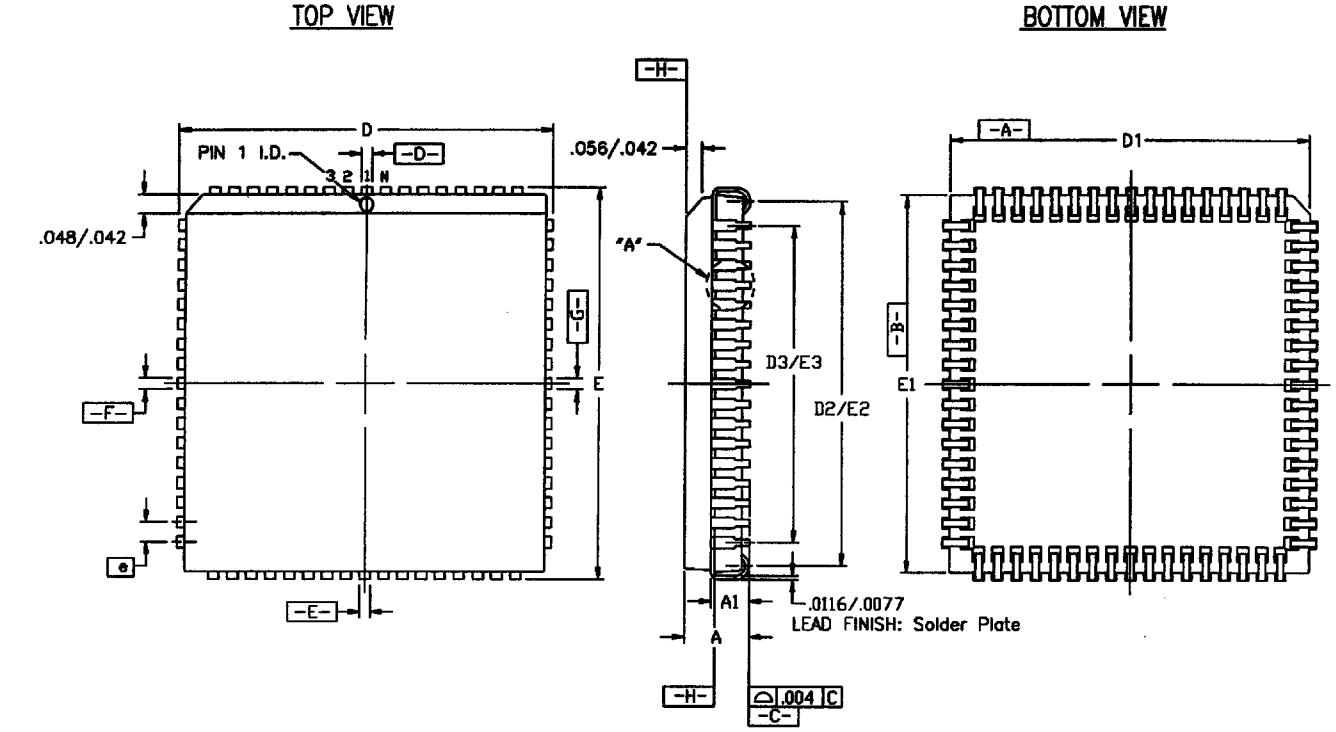
SYMBOL	SO8 INCHES MIN.	SO8 INCHES NOM.	SO8 INCHES MAX.	VO8 INCHES MIN.	VO8 INCHES NOM.	VO8 INCHES MAX.
A	.059	.064	.068			.047
A_1	.004	.006	.0098	.002	.004	.006
A_2	.055	.058	.061	.037	.039	.044
B	.013	.016	.020	.0138		.0192
C	.0075	.008	.0098	.0075		.0089
D	.189	.194	.196	.189	.194	.196
E	.150	.155	.157	.150	.155	.157
e	.050 BSC			.050 BSC		
H	.229	.236	.244	.230	.236	.244
h	.010	.013	.019	.010	.013	.019
L	.016	.025	.035	.016	.025	.035
α	0°	5°	8°	0°		8°
REF.	JEDEC MS-012					

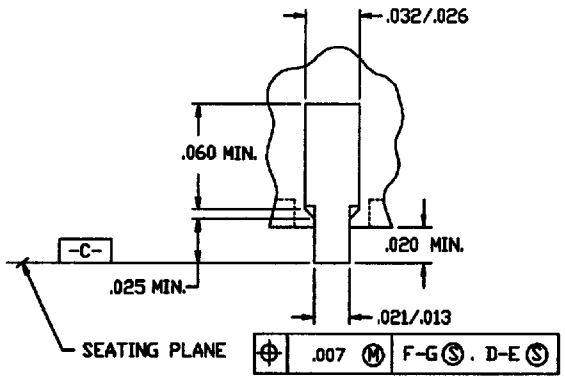
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED .006" PER SIDE.
3. DIMENSION 'E' DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED .010 INCH PER SIDE.
4. LEAD FINISH: SOLDER PLATE

8 LEAD SOIC/TSOP (SO8, VO8)

PLCC Packages - PC20, PC28, PC44, PC68, PC84





DETAIL "A"

SYMBOL	INCHES									
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
A	.165	.180	.165	.180	.165	.180	.165	.200	.165	.200
A_1	.090	.120	.099	.110	.090	.120	.090	.130	.090	.130
D/E	.385	.395	.485	.495	.685	.695	.985	.995	1.185	1.195
D_1/E_1	.350	.356	.450	.456	.650	.656	.950	.958	1.150	1.158
D_2/E_2	.290	.330	.390	.430	.590	.630	.890	.930	1.090	1.130
D_3/E_3	.200 REF.		.300 REF.		.500 REF.		.800 REF.		1.000 REF.	
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
N	20		28		44		68		84	

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS 'D1' AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE.
3. 'N' IS NUMBER OF TERMINALS.
4. CONFORM TO JEDEC MO-047
5. TOP OF PACKAGE MAY BE SMALLER THAN BOTTOM BY .010".

20, 28, 44, 68 and 84-PIN PLCC (PC20 THRU PC84)